82C711/712

Universal Peripheral Controller II

Data Sheet

January 1991

PRELIMINARY

CHIPS

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Chips and Technologies, Inc.

82C711/712
Universal Peripheral Controller II
(UPC II)

Data Sheet

(Preliminary)

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CHIPS

82C711/712
UNIVERSAL PERIPHERAL CONTROLLER II (UPC II)

82C711 Features

- For MOTHERBOARD Applications with configuration via software
- Low Power CMOS, 100 pin PQFP Package
- On Chip Power Management Features, Controllable Through Hardware and/or Software
- 100% IBM PC-XT/AT Compatibility
- 24 mA AT/XT Bus Interface Buffers
- Schmitt Trigger Input on Reset Pin and FDC interface inputs
- Two 16450 Compatible UARTs
- 1 IBM PC-XT/AT Compatible Enhanced (Bi-Directional) Parallel Port
- 24 mA Parallel Port Output Drivers
- IDE Interface (For Embedded AT & XT Hard Drives)
- Single 24 MHz Crystal/Oscillator for UART and Floppy Disk Controller
- Fully uPD72065B and IBM-BIOS Compatible Floppy Disk Controller
  - —Licensed NEC design
  - —48 mA floppy drive interface buffers
  - —Data rate and drive control registers
  - —Two pin programmable precompensation modes
  - —Supports two floppy drives directly and up to four drives with an external decoder
  - —DMA enable logic
- On-Chip Precision Analog Data Separator
  - —±380 ns at 500K bps
  - —±740 ns at 250K bps
  - —Automatically selects one of three filters
  - —Supports 250 Kb/s, 300 Kb/s, 500 Kb/s & 1 Mb/s data rates
- Member of ELEATsx CHIPSet

82C712 Features

- For ADAPTER Applications with configuration via hardware (Jumper selectable)
- Low Power CMOS, 100 pin PQFP Package
- 100% IBM PC-XT/AT Compatibility
- 24 mA AT/XT Bus Interface Buffers
- Schmitt Trigger Input on Reset Pin and FDC interface inputs
- Two 16450 Compatible UARTs
- 1 IBM PC-XT/AT Compatible Enhanced (Bi-Directional) Parallel Port
- Game Port Chip Select ($\overline{GPCS}$)
- 24 mA Parallel Port Output Drivers
- Single 24 MHz Crystal/Oscillator for UART and Floppy Disk Controller
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General Description

The 82C711/712 Universal Peripheral Controller II (UPC II) are single chip controllers offering a complete I/O solution for the PC-XT & PC-AT environments. The 82C711 and 82C712 chips are nearly operationally and pin identical.

The 82C711 supports the MOTHERBOARD application. It provides one enhanced parallel port (printer/bi-directional), two 16450 UARTs, one IDE XT/AT hard disk interface and floppy disk controller. The configuration is software controllable which can be integrated into system BIOS. Power management for the 82C711 includes modular power down for each port. The hardware management is done through the PWRGD pin. When the chip is powered down (PWRGD inactive), the current drawn is less than 250 micro amp. All inputs are disabled, and all outputs are inactive. The contents of all the registers are preserved, as long as the power supply to the 82C711 is maintained.

The 82C712 supports ADAPTER applications. It provides one printer port, two 16450 UARTs, IDE AT hard disk interface, floppy disk controller, and one game port chip select.

The 82C711/712 feature 24 mA drivers for the output buffers, including the host data bus and parallel port data bus. The floppy output drivers are capable of sinking 48 mA. The host interface is PC compatible and can be connected directly to the bus (D0–D7, A0–A9, $\overline{IOR}$, $\overline{IOW}$, AEN, IRQ3, IRQ4, FINTR, PINTR, and RESET).

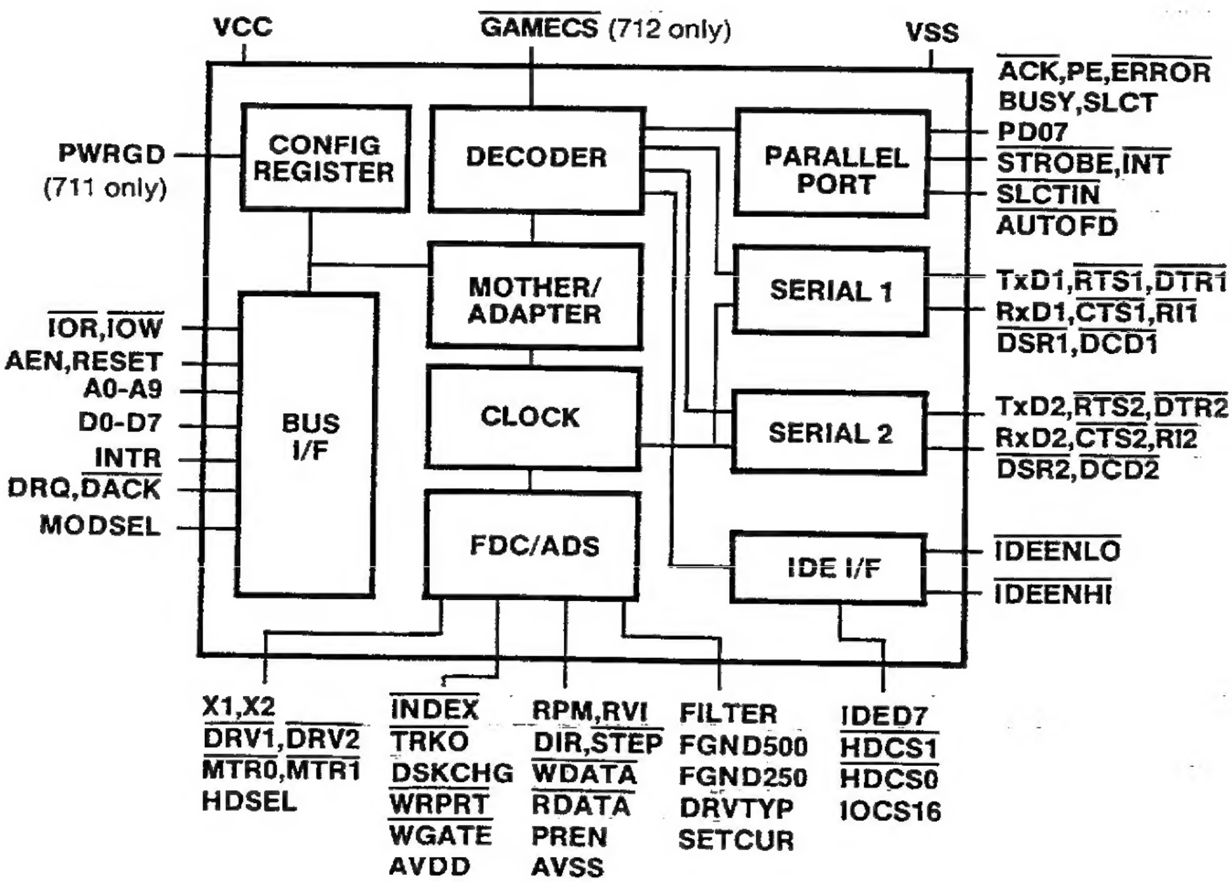
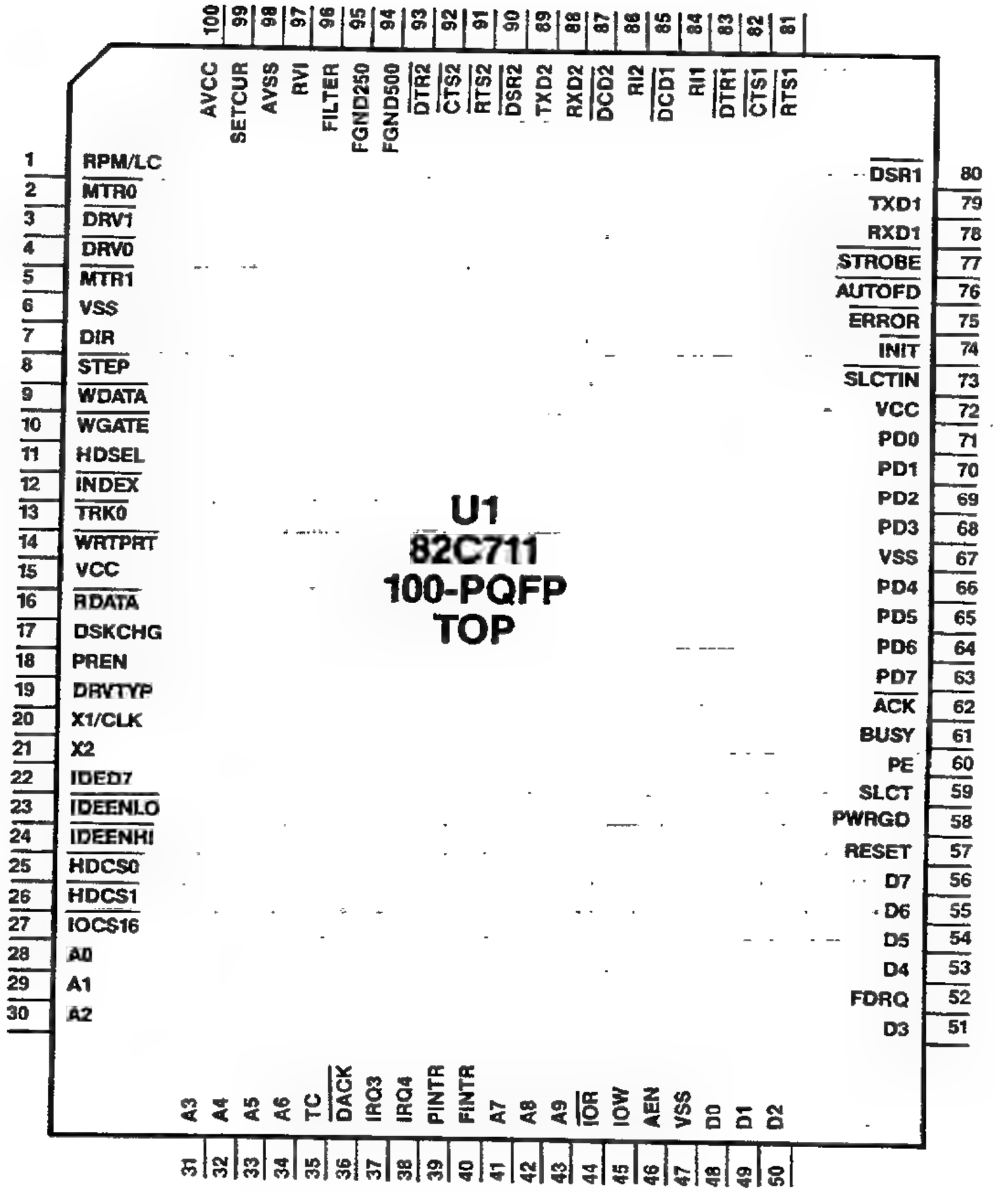
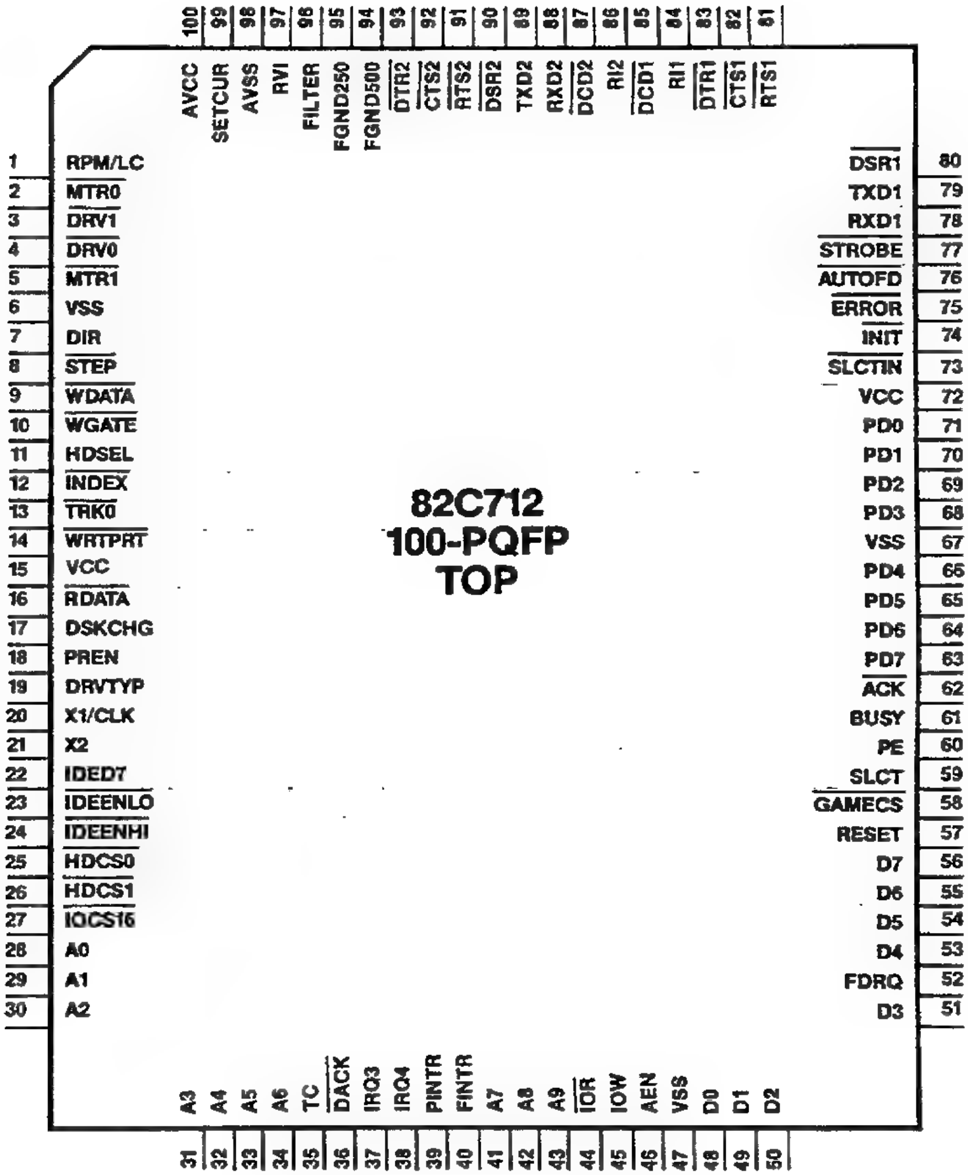


Figure 1. 82C711/712 Block Diagram.



82C711 Pin Configuration



82C712 Pin Configuration

1.0 82C711/712 Pin Description

1.1 Host Interface (29 pins)

Pin No.	Symbol	Buffer Type	Description
38	IRQ4	T	Serial Port Interrupt Request (programmable polarity), 24 mA driver. The appropriate interrupt is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after interrupt service. It is disabled through IER or hardware reset In 82C711 (MOTHERBOARD Application), IRQ4 originates from the Primary Serial Port (PSP) or Secondary Serial Port (SSP). IRQ4 is a source of PSP or SSP if their address port is programmed (by software) as COM1 or COM3.
	PSPIRQ (Primary Serial Port Interrupt)		In 82C712 (ADAPTER Application), PSPIRQ is a source of PSP interrupt. Externally, it should be connected to either IRQ3 or IRQ4 on PC/AT via jumpers.
37	IRQ3	T	Serial Port Interrupt Request (programmable polarity), 24 mA driver. The appropriate interrupt is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after interrupt service. It is disabled through IER or hardware reset. In 82C711 (MOTHERBOARD Application), IRQ3 originates from the Primary Serial Port (PSP) or Secondary Serial Port (SSP). IRQ4 is a source of PSP or SSP if their address port is programmed as COM2 or COM4.
	SSPIRQ (Secondary Serial Port Interrupt)		In 82C712 (ADAPTER Application), SSPIRQ is a source of SSP interrupt. Externally, it should be connected to either IRQ3 or IRQ4 on PC/AT via jumpers.
40	FINTR (Floppy Controller Interrupt Request)	T	Floppy Controller Interrupt Request (programmable polarity), 24 mA driver. This interrupt is enabled/disabled via bit 3 of the Drive Control Register. The active output is used to get the attention of the CPU. The required action depends on the current function of the controller.
39	PINTR (Parallel Port Interrupt Request)	T	Parallel Port Interrupt Request (programmable polarity), 24 mA driver. The interrupt is enabled/disabled via bit 4 of the Parallel Control Register. If enabled, the interrupt is generated following the $\overline{ACK}$ signal input.
28-34 41-43	A0-A9 (I/O Address)	I	Host address bit 0-9. These address bits are latched internally at the beginning of $\overline{IOR}$ or $\overline{IOW}$.
46	AEN (Address Enable)	I	Active high Address Enable indicates DMA activity. Normally, this signal is used with A0-A9, $\overline{IOW}$, $\overline{IOR}$ to decode I/O address ports.
44	$\overline{IOR}$ (I/O Read)	I	Active low I/O read from host.

1.1 Host Interface (29 pins)(Continued)

Pin No.	Symbol	Buffer Type	Description
45	$\overline{\text{IOW}}$ (I/O Write)	I	Active low I/O write from host.
57	RESET (Master Reset)	IS	Active high Reset from host (Schmitt-trigger input). RESET has to be valid for a minimum of 500 nanosecond. The effect of hardware reset is shown in the functional description of each port. The configuration registers are not affected. They come up in the default condition only on power up. In 82C712 (ADAPTER Application) the falling edge of RESET will latch the jumper configuration. The Jumper Select pin must be valid prior to this edge.
48-51 53-56	D0-D7 (Data Bus)	I/OH	Host data bus, 24 mA driver. This bi-directional data bus is used to transfer information between the CPU and the 82C711/712.
36	$\overline{\text{DACK}}$ (DMA Acknowledge)	I	Active low input to acknowledge the DMA request. This signal normally is used to enable DMA read or write.
52	FDRQ (FDC DMA Request)	OH	Active high DMA request output signal to the host, 24 mA driver.
35	TC (Terminal Count)	I	Active high input signal indicates termination of DMA transfer, qualified by $\overline{\text{DACK}}$ before use on chip.

1.2 Parallel Port Controller (17 pins):

Pin No.	Symbol	Buffer Type	Description
71-68 66-63	PD0-PD7 (Port Data)	I/OH	The bi-directional parallel data bus is used to transfer information between CPU and peripherals. These signals have high current drive and capable of sinking 24 mA @ 0.5V
77	$\overline{\text{STROBE}}$ (Data Strobe)	OC	This active low output indicates to the peripheral that the data at the parallel port is valid. This pin has high current drive and is capable of sinking 24 mA @ 0.5V.
73	$\overline{\text{SLCTIN}}$ (Select Input)	OC	This active low output selects the printer when it is low. This pin has high current drive and is capable of sinking 24 mA @ 0.5V.
74	$\overline{\text{INIT}}$ (Initialize)	OC	This active low output initializes (resets) the printer when it is low. This pin has high current drive and is capable of sinking 24 mA @ 0.5V.
76	$\overline{\text{AUTOFD}}$ (Automatic Feed)	OC	When this output is low the printer automatically adds one line feed after each line is printed. This pin has high current drive and is capable of sinking 24 mA @ 0.5V.
62	$\overline{\text{ACK}}$ (Acknowledge)	I	Active low Acknowledge input. Low indicates that data has been received and the printer is ready to accept more data.
61	BUSY (Printer Busy)	I	Active high Busy input. The high input signal indicates the printer can not accept additional data.

1.2 Parallel Port Controller (17 pins)(Continued)

Pin No.	Symbol	Buffer Type	Description
60	PE (Paper End)	I	Active high Paper End input. The high input signal indicates the printer is out of paper.
59	SLCT (Select)	I	Active high device Select input. The input is set high by the printer when it is selected.
75	$\overline{\text{ERROR}}$ (Error)	I	Active low Error input. This input is set low by the printer when it detects the error.

1.3 Serial Port Interface (10 Pins):

Pin No.	Symbol	Buffer Type	Description
82, 92	$\overline{\text{CTS1}}$, $\overline{\text{CTS2}}$ (Clear to Send)	I	Active low Clear to Send inputs for Primary and Secondary serial ports. Handshake signal which notifies the UART that the MODEM is ready to receive data. The CPU can monitor the status of $\overline{\text{CTS}}$ signal by reading bit 4 of Modem Status Register (MSR). A CTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{CTS}}$ changes state. The $\overline{\text{CTS}}$ signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of $\overline{\text{CTS}}$.
80, 90	$\overline{\text{DSR1}}$, $\overline{\text{DSR2}}$ (Data Set Ready)	I	Active low Data Set Ready inputs for Primary and Secondary serial ports. Handshake signal which notifies the UART that the MODEM is ready to establish the communication link. The CPU can monitor the status of $\overline{\text{DSR}}$ signal by reading bit 5 of Modem Status Register (MSR). A $\overline{\text{DSR}}$ signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{DSR}}$ changes state. Note: Bit 5 of MSR is the complement of DSR.
85, 87	$\overline{\text{DCD1}}$, $\overline{\text{DCD2}}$ (Data Carrier Detect)	I	Active low Data Carrier Detect input for Primary and Secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the MODEM. The CPU can monitor the status of $\overline{\text{DCD}}$ signal by reading bit 7 of Modem Status Register (MSR). A $\overline{\text{DCD}}$ signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{DCD}}$ changes state. Note: Bit 7 of MSR is the complement of $\overline{\text{DCD}}$.
84, 86	$\overline{\text{RI1}}$, $\overline{\text{RI2}}$ (Ring Indicator)	I	Active low Ring Indicator input for Primary and Secondary serial ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the MODEM. The CPU can monitor the status of $\overline{\text{RI}}$ signal by reading bit 6 of Modem Status Register (MSR). A $\overline{\text{RI}}$ signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{RI}}$ changes state. Note: Bit 6 of MSR is the complement of $\overline{\text{RI}}$.
78, 88	RXD1, RXD2 (Receive Data)	I	Active high receive serial data input from communication link.

1.3 Serial Port Interface (10 pins)(Continued)

Pin No.	Symbol	Buffer Type	Description
81	$\overline{RTS1}$ (Request To Send)	O	Active low Request To Send output for Primary serial port. Handshake output signal notifies MODEM that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the $\overline{RTS}$ signal to inactive mode (high). Forced inactive during loop mode operation.
	PCF1	I	Parallel Port Configuration Control 1 in 82C712 (ADAPTER Application). Input during hardware RESET to select address for parallel port. (NOTE 1)
91	$\overline{RTS2}$ (Request To Send)	O	Active low Request To Send output for Secondary serial port. Handshake output signal notifies MODEM that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the $\overline{RTS}$ signal to inactive mode (high). Forced inactive during loop mode operation.
	S2CF0	I	Secondary Serial Port Configuration Control 0 in 82C712 (ADAPTER Application). Input during hardware RESET to select address for secondary serial port. (NOTE 1)
83	$\overline{DTR1}$ (Data Terminal Ready)	O	Active low Data Terminal Ready output for Primary serial port. Handshake output signal notifies MODEM that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the $\overline{DTR}$ signal to inactive mode (high). Forced inactive during loop mode operation.
	IDECF	I	IDE configuration control in 82C712 (ADAPTER Application). Input during hardware RESET to enable/disable IDE. (NOTE 1)
93	$\overline{DTR2}$ (Data Terminal Ready)	O	Active low Data Terminal Ready output for Secondary serial port. Handshake output signal notifies MODEM that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the $\overline{DTR}$ signal to inactive mode (high). Forced inactive during loop mode operation.
	S2CF1	I	Secondary Serial Port Configuration Control 1 in 82C712 (ADAPTER Application). Input during hardware RESET to select address for Secondary serial port. (NOTE 1)
79	TXD1 (Transmit Data)	O	Active high transmit serial data output to the communication link for Primary serial port.
	PCF0	I	Parallel Port Configuration Control 0 in 82C712 (ADAPTER Application). Input during hardware RESET to select address for parallel port. (NOTE 1)

1.3 Serial Port Interface (10 pins) (Continued)

Pin No.	Symbol	Buffer Type	Description
89	TXD2 (Transmit Data)	O	Active high transmit serial data output to the communication link for Secondary serial port.
	FDCCF	I	FDC Configuration control in 82C712 (ADAPTER Application). Input during hardware RESET to enable/disable FDC. (NOTE 1)
1.4 IDE Interface (6 Pins):			
27	$\overline{\text{IOCS16}}$ (16 bit I/O Indication)	I	Active low 16 bit I/O indication while in the AT hard disk mode. The hard disk interface generates $\overline{\text{IOCS16}}$ to inform the host and the 82C711/712 that 16 bit I/O transfers are about to begin. $\overline{\text{IOCS16}}$ is active only when transferring data words in AT mode. Low = 16 bit, high = 8 bit (AT mode).
	$\overline{\text{HDACK}}$	I	Active Low HDC DMA Acknowledge while in the XT hard disk mode. XT mode is not available in 82C712 (ADAPTER Application).
22	IDED7 (IDE Data Bit 7)	I/OH	IDE Data Bit 7 while in the AT hard disk mode. IDED7 transfers data at I/O addresses 1F0H-1F7H (R/W), 3F6H (R/W), 3F7(W). IDED7 should be connected to the IDE data bit 7. Normally, the 82C711/712 functions as a buffer, transferring data bit 7 between the IDE device and the host. During read of I/O address 3F7H, IDED7 is FDC Disk Change bit 7. In the XT hard disk mode, IDE7 is not used.
25	$\overline{\text{HDCS0}}$ (Hard Disk Chip Select 0)	OH	Active low Hard Disk Chip Select 0 for IDE interface in either AT/XT hard disk modes. This decodes the address space 1F0H-1F7H (default) if configured in AT mode (CR#00H<1> = 1) or 320H-323H if configured in XT mode (CR#00H<1> =0).
26	$\overline{\text{HDCS1}}$ (Hard Disk Chip Select 1)	OH	Active low Hard Disk Chip Select 1 for IDE interface, in either AT/XT hard disk modes. This decodes the address space 3F6-3F7H.
24	$\overline{\text{IDEENHI}}$ (High Data Buffer Enable)	O	Active low High Data Buffer Enable while in the AT hard disk mode. $\overline{\text{IDEENHI}}$ is active only when $\overline{\text{IOCS16}}$ is active, I/O address 1F0H-1F7H, and AT mode is selected. $\overline{\text{IDEENHI}}$ is not used in the XT hard disk mode.
	S1CF0		Primary Serial configuration 0 in 82C712 (ADAPTER Application). Input during hardware RESET to select address for secondary serial port. (NOTE 1)
23	$\overline{\text{IDEENLO}}$ (Low Data Buffer Enable)	O	Active low Low Data Buffer Enable while in either AT/XT hard disk modes. $\overline{\text{IDEENLO}}$ is active when accessing I/O address 1F0H-1F7H and 3F6H-3F7H (AT mode) or 320H-323H (XT mode: 8 bit DMA or programmed I/O).
	S1CF1		Primary Serial configuration 1 in 82C712 (ADAPTER Application). Input during hardware RESET to select address for secondary serial port. (NOTE 1)

1.5 Floppy Interface (24 pins)

Pin No.	Symbol	Buffer Type	Description
16	$\overline{\text{RDATA}}$ (Read Data)	IS	The active low signal reads raw data from the disk. This is a Schmitt input.
9	$\overline{\text{WDATA}}$ (Write Data)	OD	This active low signal writes precompensated serial data to the selected drive. This is a high open current drain output and is not gated internally with the Write gate.
4, 3	$\overline{\text{DRV0, 1}}$ (Drive)	OD	These active open drain outputs select drives 0-3. Two drives can be supported directly. An external decoder (2 to 4) is needed to select four drives.
17	DSKCHG (Disk Change)	IS	This Diskette Change signal notifies the FDC that the disk drive door has been opened. This Schmitt latched input is inverted and read via bit 7 of I/O address 3F7H.
10	$\overline{\text{WGATE}}$ (Write Gate)	OD	This active low open drain signal enables the head to write onto the disk.
7	DIR (Direction)	OD	This open drain output signal controls the head movement direction. (Low = Step in; High = Step out)
8	$\overline{\text{STEP}}$	OD	This active low output signal supplies the step pulse, at a programmable rate, to move the head for seek operation.
11	HDSEL (Head Select)	OD	This open drain output selects the head on the selected drive. (Low = side 0; High = side 1)
13	$\overline{\text{TRK0}}$ (Track 0)	IS	This active low Schmitt input indicates that the head is in track 0 of the selected drive.
14	$\overline{\text{WRPRT}}$ (Write Protect)	IS	This active low Schmitt input indicates that the disk is write-protected. Any Write command is ignored.
12	$\overline{\text{INDEX}}$	IS	This active low Schmitt input indicates the beginning of a track.
2, 5	$\overline{\text{MTR0, 1}}$ (Motor)	OD	This active low open drain output selects motor drivers 0-3. Two drivers are supported directly. An external decoder (2 to 4) is needed to select four motor drivers. The motor enable bits are software controllable via the Digital Output Register (DOR).
96	FILTER	I/O	This signal is the output of the charge pump and the input to the VCO. PLL filter circuitry is connected to this pin (FGND250, FGND500 and analog ground).
94	FGND500 (Filter Ground 500 Kb/s)	OL	This low impedence output signal is connected to 500 Kb/s (MFM) PLL filter circuitry.
95	FGND250 (Filter Ground 250 Kb/s)	OL	This low impedence output signal is connected to 250 Kb/s (MFM) PLL filter circuitry.
18	PREN (Precompensation Enable)	I	This input selects precompensation mode: Low = Normal, High = Alternate. Precompensation values (shown in Floppy section) depend on the selected data rate and precompensate mode.

1.5 Floppy Interface (24 pins)(Continued)

Pin No.	Symbol	Buffer Type	Description
19	DRVTYP (Drive Type)	I	When this input is low, the dual speed spindle motor driver is used. If 300Kb/s is selected via Data Rate register, the PLL actually runs at 250Kb/s. When this input is high (standard AT), the single speed spindle motor driver is used. The PLL runs at 300Kb/s when data rate is selected at 300Kb/s.
99	SETCUR (Set Current)	I	This signal is connected to the Analog ground via an external resistor to set the charge pump current for PLL filter.
1	RPM/LC (Revolutions per Minute/Low current)	OD	Depending on DRVTYP input, this open drain output signal can function in two modes: 1. When DRVTYP is LOW (dual speed spindle), this output selects either 300RPM or 360RPM. This output is low when 250/300Kb/s is selected and high when 500Kb/s selected. 2. When DRVTYP is HIGH (single speed spindle), the output goes high when 500Kb/s is selected (high density media). It is also used to indicate when to reduce write current.
97	RVI	I	An external resistor connects this pin to Analog ground for PLL filter.

1.6 Power and Ground (10 pins)

Pin No.	Symbol	Buffer Type	Description
15, 72	Vcc (2) (Power)		+5VDC Digital supply .
20	X1/CLK (Crystal Clock)	Iclk	The external connection for series resonant 24 MHz crystal input. A CMOS compatible oscillator is required if a crystal is not used.
21	X2 (Crystal)	O	24 MHz crystal. If an external clock is used, this pin should not be connected.
58	PWRGD (Power Good)	I	Active high Power Good indication in 82C711 (MOTHERBOARD Application). The 82C711 is fully functional when PWRGD is active. When PWRGD is inactive and Vcc is still valid, the 82C711 is isolated from the rest of the circuit. All accesses are ignored, all inputs are disabled, and all outputs are tri-stated. However, contents of all registers are preserved, and the current drain drops to standby current (Istby). An internal weak pull-up resistor is attached to this pin.
	$\overline{\text{GAMECS}}$	O	In 82C712 (ADAPTER Application) this pin is $\overline{\text{GAMECS}}$ output (no standby mode feature in ADAPTER MODE). It will be low when I/O address 201H is selected.
6, 47, 67	Vss (3) (Ground)		0V Reference for the FDC digital, CPU interface, serial ports, parallel port, and disk interface output drive circuitry, respectively.
100	AVcc (Analog Power)		Analog +5VDC for the PLL.

1.6 Power and Ground (10 pins)(Continued)

Pin No.	Symbol	Buffer Type	Description
98	AVss (Analog Ground)		Analog Ground for the PLL.

Buffer Types:

I = TTL input
IS = Schmitt-trigger input
O = TTL output
OH = High current TTL output
OC = Open Drain
OD = High current open drain output
OL = Low current open drain output
T = Tri-state TTL output, 24 mA
Iclk = Clock Input

NOTE 1: The external 27K ohm resistor is used to pull these pins to the required signal levels.

2.0 SERIAL PORT (UART)

2.1 Introduction

Two equivalent NS16450 UARTs are implemented on the 82C711/712. The serial port is fully compatible to the 16450 ACE registers. The programmable features allow data rates ranging from 50 baud to 115.2 Kbaud; 5 to 8 bit character size with 1 start and 1, 1.5, 2 stop bits; even, odd, sticky, or no parity; and prioritized interrupts. An interrupt from the UART is enabled or disabled (tri-stated) using the OUT2 bit. If a 1 is written to OUT2, UART, interrupt is enabled. Writing 0 tri-states the interrupt. The primary serial port base address is programmed via bit 0 and 1 of Configuration Register 2. The secondary serial port base address is programmed via bits 4 and 5 of Configuration Register 2. An on-chip baud rate generator divides the input clock or crystal frequency by a number from 1 to 65535. This frequency is used for both receiving and transmitting serial data.

Serial-to-parallel conversion is performed on received data and parallel-to-serial conversion is performed on transmitted data. Status of the UART is available at any time. To access it, the CPU reads the appropriate status register in the 82C711/712. The current state and type of a transfer are contained in this status information as are details regarding any errors encountered. The conditions under which the processor will be interrupted and the interrupt line to be used are programmable.

Control lines are provided to permit interfacing to a MODEM. Internal diagnostics are supported that permit simulation of break, parity, overrun and framing error conditions as well as operation in loopback mode.

2.2 Serial Port Registers

The following sections describe the details of serial ports. Since the function of two serial ports are identical, the descriptions apply for both of them.

Addressing of the accessible UART registers is shown in Table 2.0 below. The base address of all registers is software programmable during the configuration sequence (see the section entitled "82C711/712 Configuration"). UART registers are located at sequentially increasing addresses above this base address. The 82C711/712 contains two UARTs which contain a set of the registers described below.

Table 2.0 Addressing of UART Registers

DRAB	A2	A1	A0	Offset	Register Name
0	0	0	0	0H	Received Buffer Register (R)
0	0	0	0	0H	Transmit Buffer Register (W)
0	0	0	1	1H	Interrupt Enable Register (R/W)
X	0	1	0	2H	Interrupt Flag Register (R/W)
X	0	1	1	3H	Byte Format Register (R/W)
X	1	0	0	4H	Modem Control Register (R/W)
X	1	0	1	5H	Line Status Register (R/W)
X	1	1	0	6H	Modem Status Register (R/W)
X	1	1	1	7H	Scratch Pad Register (R/W)
1	0	0	0	0H	Divisor LSB (R/W)
1	0	0	1	1H	Divisor MSB (R/W)

Where:

X = Don't Care
MSB = Most Significant Byte
LSB = Least Significant Byte
DRAB = Divisor Register Address Bit (Bit 7 of Byte Format Register)

BIT DEFINITIONS OF SERIAL PORT REGISTERS

2.2.1 *Receive Buffer (RB)* *Offset = 0H, Read only, DRAB = 0*

This register holds the incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Double buffering is supported by the 82C711/712. This scheme uses an additional shift register (the Receive Shift Register; not user accessible) to assemble the incoming byte before it is loaded into the Receive Buffer.

2.2.2 *Transmit Buffer (TB)* *Offset=0H, Write only, DRAB=0*

This register holds the data byte to be sent. Bit 0 is the least significant bit, which is transmitted and received first. Double buffering is supported by the 82C711/712. This scheme uses a shift register (the Transmit Shift Register; not user accessible) which is loaded from the Transmit Buffer. The transmitted byte is then shifted out of the Transmit Shift Register to the TXD pin.

2.2.3 *Interrupt Enable Register (IER)* *Offset=1H, Read/Write, DRAB = 0*

The low order 4 bits of this register control the enabling of each of the four possible types of interrupts. Setting a bit to a logic 1 enables the corresponding interrupt. It is possible to enable all, none, or some of the interrupt sources. Disabling all interrupts means that the interrupt flag register content is not valid and that none of the interrupt signals output by the 82C711/712 can be triggered by a UART. All other portions of the UART are unaffected by the disabling of interrupts. The individual bit definitions are as follows:

Bit 0: A logic 1 here causes an interrupt when the Receive Buffer contains valid data.

Bit 1: A logic 1 here causes an interrupt when the Transmit Buffer is empty.

Bit 2: A logic 1 here causes an interrupt when an error (Overrun, Parity, Framing or Break) has been encountered. The Line Status register must be read to determine the type of error.

Bit 3: A logic 1 here causes an interrupt when one of the bits in the MODEM Status register changes state.

Bits 4-7: These four bits are set to 0.

2.2.4 *Interrupt Flag Register (IFR)* *Offset = 2H, Read/Write, DRAB = X*

When accessed, this register reports the highest pending interrupt. By reading it, the CPU can determine the source of the interrupt and can act accordingly. The Interrupt Flag Register (IFR) records the highest pending interrupt in bits 0 through 2. Other interrupts are temporarily disregarded (they are internally saved by the 82C711/712) until the highest priority one is serviced.

Four levels of prioritized interrupts exist. In descending order of priority they are:

1. Line Status (highest priority)
2. Receive Buffer full
3. Transmit Buffer empty
4. MODEM Status (lowest priority)

Bit definitions for the IFR are as follows:

Bit 0: If this bit is a zero, an interrupt is pending and bits 1 and 2 can be read to determine the source of the interrupt. When this bit is a logic 1, no interrupts are pending. Note that this bit can be used in a polled environment to determine if an interrupt is pending. It can also be used for the same purpose with a hardwired interrupt priority scheme. In the latter case, bits 1 and 2 of this register act as a pointer to an interrupt service routine.

Bits 1 and 2: As indicated in Table 2.1, these two bits specify the type and source of the interrupt.

Bits 3-7: These five bits are set to 0.

2.2.5 Byte Format Register (BFR)
Offset = 3H, Read/Write, DRAB = X

This read/write register contains format information for the serial line. Since it can be read, a separate copy of its content need not be kept in system memory. Bit definitions are as follows:

Bits 0 and 1: These specify the word length for received and transmitted characters. Start, stop and parity bits are not included in the word length value. The word lengths are:

Bit 0	Bit 1	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: The combination of this bit and Bits 0 and 1 of this register determine the number of stop bits used with each transmitted character. The table below summarizes this information. Note that the receiver will ignore additional stop bits beyond the first regardless of the number of stop bits used when transmitting.

Bit 2	Word Length	Number of Stop Bits
0	—	1
1	5 Bits	1 1/2
1	6 Bits	2
1	7 Bits	2
1	8 Bits	2

Bit 3: A logic 1 in this bit enables parity generation (during transmission) and checking (during receipt). The parity bit is always after the last data bit but before the first stop bit. If enabled, a parity bit of the proper state (0 or 1) is generated such that the sum (carry ignored) of all data bits plus the parity bit produces either an even (even parity) or odd (odd parity) value.

Bit 4: This Even Parity bit controls parity sense. It is ignored unless Bit 3 is a logic 1. If Bits 3 and 4 are logic 1s (even parity), an even number of logic 1s will be transmitted and a parity error will be generated each time an odd number is received. If Bit 3 is a 1 and Bit 4 is a 0 (odd parity), an odd number of logic 1s will be transmitted and a parity error will be generated each time an even number is received.

Bit 5: This is the Force Parity bit. It ensures that the parity bit and sense (even or odd) match regardless of the sum normally used to determine parity. Thus if BFR Bits 3, 4 and 5 are all logic 1s (even parity), the parity bit transmitted will always be a 0 and a parity error will be detected if a logic 1 parity bit is received. If Bits 3 and 5 are 1 and Bit 4 is 0, the parity bit transmitted will always be a 1 and a parity error will be detected if a 0 parity bit is received.

Bit 6: This BREAK bit, when set to a logic 1, forces the transmitted data output pin TXD to a Spacing or logic 0 condition. This BREAK condition is terminated when Bit 6 is set to a 0. The operation of the transmitter logic is unaffected by the value of this bit; only the value of the TXD pin is affected. A BREAK condition is typically used to alert a terminal in a communications system. To prevent the transmission of erroneous data, follow the steps below:

1. Load a NULL character (all zeroes) into the Transmit Buffer.
2. Load Bit 6 (BREAK bit) after the next Transmit Buffer Empty (TBE) occurs.
3. Time the length of the BREAK condition by continuing to load NULL characters into the Transmit Buffer and counting the number loaded.
4. Clear the BREAK condition only after a Transmitter Empty (TEMT) condition occurs.

Bit 7: This Divisor Register Address Bit (DRAB) must be a logic 1 to permit access to the Divisor Registers. Access to all other internal UART registers requires that this bit be 0.

2.2.6 *Modem Control Register (MCR)*

Offset = 4H, Read/Write, DRAB = X

This byte-wide register is used to manage the connection to an external MODEM or data set. Bit definitions are as follows:

Bit 0: This $\overline{DTR}$ bit determines the state of the $\overline{DTR}$ output pin. Setting Bit 0 to a logic 1 forces $\overline{DTR}$ to its active state (logic 0). If Bit 0 is a logic 0, $\overline{DTR}$ will be inactive (logic 1). An external inverting buffer is typically used (to insure the proper polarity of $\overline{DTR}$) when connecting a 82C711/712 $\overline{DTR}$ output to a MODEM or data set.

Bit 1: This $\overline{RTS}$ bit determines the state of the corresponding $\overline{RTS}$ 82C711/712 output pin in a fashion identical to Bit 0 (see above).

Bit 2: This bit is used to control the OUT1 bit. It does not have an output pin associated with this bit. It can be read or written by CPU.

Note: OUT1 is an internal chip signal.

Bit 3: This bit is used to enable an interrupt (OUT2 pin of UART). When OUT2 = 0 (default), the serial interrupt is forced into high impedance. When OUT2 = 1 the serial interrupt output is enabled.

Note: OUT2 is an internal chip signal.

Bit 4: This Loopback bit is used for self-diagnostic purposes. If it is a logic 1:

1. The TXD 82C711/712 output pin is set to a logic 1 (Marking state) and it is disconnected from the output of the Transmit Shift Register.
2. The RXD 82C711/712 input pin is disconnected from the Receive Shift Register.
3. The input to the Receiver Shift Register is internally connected to the output of the Transmit Shift Register.
4. All MODEM control input pins ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected from the internal circuitry.
5. MODEM control output pins $\overline{DTR}$ and $\overline{RTS}$ are forced to their inactive state (logic 1).
6. MODEM control output $\overline{DTR}$ is connected internally to MODEM control input $\overline{DSR}$, MODEM control output $\overline{RTS}$ is internally connected to input $\overline{CTS}$, and MODEM Control Register (MCR) bit 2 determines the state of bit 6 of the MODEM Status Register (MSR). Bit 3 of the MCR controls bit 7 of the MSR.
7. Data which is transmitted will immediately be received, permitting the CPU to verify the data paths internal to the 82C711/712 and its connection to the CPU.

While operating in diagnostic loopback mode, interrupts are disabled. Interrupts are controlled by the Interrupt Enable register. Interrupts which are due to MODEM signals operate as documented, although the source is now the lower 4 bits of the MODEM Control Register rather than the MODEM input pin signals.

Bits 5, 6 and 7: These bits are set to 0.

Table 2.1 UART Interrupt Specifications (Interrupt Flag Register)

Bit 2	Bit 1	Bit 0	Priority	Type	Source	Servicing The Interrupt
0	0	1		NO INTERRUPT PENDING		
1	1	0	Highest	Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Read Line Status Register
1	0	0	Second	Receive Buffer Full	Receive Data	Read Receive
0	1	0	Third	Transmit Buffer Empty	Transmit Buffer	Read IFR or Write transmit buffer
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Carrier Detect	Read MODEM Status Register

2.2.7 *Line Status Register (LSR)* *Offset = 5H, Read Only, DRAB = X*

This byte-wide register supplies serial link status information to the CPU. A Receive Line Status interrupt is caused by one of the conditions flagged by Bits 1 through 4 of this register. It is read only. Writes to it are used at the factory for testing purposes and are not recommended. Bit definitions are as follows:

Bit 0: This Receive Buffer Full (RBF) bit is set to a logic 1 when an incoming character has been transferred from the Receive Shift Register to the Receive Buffer. Reading the Receive Buffer resets it to a logic 0.

Bit 1: This Overrun Error bit is set to a logic 1 when a new character is transferred into the Receive Buffer before the previously received character was read by the CPU. The previously received character is lost. When the CPU reads the LSR, the Overrun Error bit is reset to a 0.

Bit 2: This Parity Error bit is set to a logic 1 whenever a parity error is detected (received character has a parity other than that selected). Reading the LSR resets this bit to a 0.

Bit 3: This Framing Error bit is set to a logic 1 when an incoming character has no stop bit after the last data bit or (if parity is enabled) after the parity bit. A valid stop bit is the presence of a Mark condition (logic 1) in the proper time slot after the last data bit or the parity bit. Reading the LSR resets this bit to a 0.

Bit 4: This Break Interrupt bit will be a logic 1 if a Space condition (logic 0) is present on the RXD line for an entire character time (start bit time, plus data bit time, plus parity bit time, plus stop bit time). Reading the LSR resets this bit to a 0.

Bit 5: This Transmit Buffer Empty (TBE) bit is set to a logic 1 when an outgoing character is loaded from the Transmit Buffer (TB) into the Transmit Shift Register. If the TBE interrupt is enabled, an interrupt will be generated when this bit is set. Writing a character to the TB resets this bit to a 0.

Bit 6: This Transmitter Empty (TEMT) bit will be set to a logic 1 when both the Transmit Buffer and the Transmit Shift Register are empty. When either of these two registers contains a character, this bit will be reset to a 0.

Bit 7: This bit is set to 0.

2.2.8 *MODEM Status Register (MSR)* *Offset = 6H, Read/Write, DRAB = X*

This byte-wide register holds the current value of the MODEM control lines. It also sets a bit (to a logic 1) each time one of these control lines

changes state. Reading the MSR resets all of the Change bits to 0. A MODEM Status Interrupt is generated (if it is enabled) when Bit 0, 1, 2 or 3 is set to a 1. Bit definitions are:

Bit 0: This is the Clear To Send Changed bit. It is set to a 1 if the $\overline{CTS}$ line has changed state since the last time the MSR was read.

Bit 1: This is the Data Set Ready Changed bit. It is set to a 1 if the $\overline{DSR}$ line has changed state since the last time the MSR was read.

Bit 2: This is the Rising Edge of Ring Indicator bit. It is set to a 1 if the $\overline{RI}$ line has changed from a logic 0 to a logic 1 since the last time the MSR was read.

Bit 3: This is the Data Carrier Detect Changed bit. It is set to a 1 if the $\overline{DCD}$ line has changed state since the last time the MSR was read.

Bit 4: This is the Clear To Send bit. It is the complement of the $\overline{CTS}$ pin. When in diagnostic loopback mode, this bit is identical to the $\overline{RTS}$ bit in the MODEM Control Register (MCR).

Bit 5: This is the Data Set Ready bit. It is the complement of the $\overline{DSR}$ pin. When in diagnostic loopback mode, this bit is identical to the $\overline{DTR}$ bit in the MCR.

Bit 6: This is the Ring Indicator bit. It is the complement of the $\overline{RI}$ pin. In diagnostic loopback mode, it is controlled by Bit 2 of the MCR.

Bit 7: This is the Data Carrier Detect bit. It is the complement of the $\overline{DCD}$ pin. In diagnostic loopback mode, it is controlled by Bit 3 of the MCR.

2.2.9 *Scratchpad Register*
Offset = 7H, Read/Write, DRAB = X

This byte-wide register has no effect on the UART within which it is located. It can be used for any purpose by the programmer.

2.3 Effects of Hardware Reset

Table 2.2 below details the effect of a hardware RESET on the UART located in a 82C711/712

Table 2.2 Action of a Hardware Reset on the 82C711/712 UART

Register or Signal	Cause of Reset	Reset State
Interrupt Enable Register	Hardware RESET	All bits = logic 0
Interrupt Flag Register	Hardware RESET	Bit 0 = logic 1 Other bits = logic 0
Byte Format Register	Hardware RESET	All bits = logic 0
MODEM Control Register	Hardware RESET	All bits = logic 0
Line Status Register	Hardware RESET	Bits 5, 6 = logic 1 Other bits = logic 0
MODEM Status Register	Hardware RESET	Bits 0-3 = logic 0 Bits 4-7 = Input Signal
TXD2 and TXD1	Hardware RESET	logic 1 (high)
Receive Line Status Interrupt	Hardware RESET or Read LSR	logic 0 (low)
Receive Buffer Full Interrupt	Hardware RESET or Read RB	logic 0 (low)
Transmit Buffer Empty Interrupt	Hardware RESET or Read TB	logic 0 (low)
MODEM Status Interrupt	Hardware RESET or Read MSR	logic 0 (low)
$\overline{RTS2}$ and $\overline{RTS1}$	Hardware RESET	logic 1 (high)
$\overline{DTR2}$ and $\overline{DTR1}$	Hardware RESET	logic 1 (high)

2.4 Baud Rate Generation

The UART contains a programmable Baud Generator. The 24 MHz crystal oscillator frequency input is divided by 13 to provide a frequency of 1.8462 MHz. This is sent to the Baud Rate Generator and divided by the divisor for the UART. The output frequency of the Baud Rate Generator is 16 x the baud rate, [(divisor # = (frequency input) ÷ (baud rate x 16)]. The output of the Baud Rate Generator drives the transmitter and receiver sections of the serial channel. Two 8-bit latches store the divisor in a 16-bit binary format. This Divisor Latch must be loaded during initalization to ensure proper operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud Counter is loaded.

Table 2.3 lists decimal divisors to use with a crystal frequency of 24 MHz. The oscillator input to the chip should always be 24 MHz to ensure that the Floppy Disk Controller timing is accurate and that the UART divisors are compatible with existing software. Using a divisor of zero is not recommended.

Table 2.3 Divisors, Baud Rates and Clock Frequencies

	1.8462 MHz Clock	
Divisor Baud Rate	**Decimal Divisor for 16 X Clock**	**Percent Error (Note 1)**
50	2304	0.001
75	1536	
110	1047	
134.5	857	0.004
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.005
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	0.030
115200	1	

Note 1: The percent error for all Baud Rates, except where indicated otherwise, is 0.002%.

3.0 PARALLEL PORT

3.1 Introduction

The Parallel Port is compatible to the IBM XT/AT Parallel Port, plus, in the MOTHERBOARD (82C711) mode only, a PS/2-like extended mode for bi-directional mode. When the parallel port is disabled via the configuration register, all outputs are disabled, and register contents are preserved. Upon power up, the control signals are inactive. The status register reflects the status signals.

3.2 Printer Interface Accessible Registers

Table 3.1 depicts the registers and I/O ports which are accessible for the parallel printer port. These are compatible with the IBM PC parallel port. Bit definitions for each of these registers are given after the diagram. All addresses for the parallel port are offsets from the base address specified during the 82C711/712 configuration process.

3.2.1 *Data Latch (Port A)*

Offset = 00H

This read/write register is located at an offset of 0H from the base address of the parallel port. Data written to this register is transmitted to the printer. Data read from this port is the data which is on the connector. This port is 100% compatible with the IBM PC-AT parallel port.

3.2.2 *Printer Status Register (Port B)*

Offset = 01H

This read-only register is located at an offset of 1H from the base address of the parallel port. Bit definitions are as follows:

Bit 7: $\overline{\text{Busy}}$. This bit reflects the state of the 82C711/712 BUSY input pin. A 0 means that the printer is busy and cannot accept data. A 1 indicates that the printer is ready to accept data.

Bit 6: $\overline{\text{ACK}}$. This bit reflects the state of the $\overline{\text{ACK}}$ input pin. A 0 means that the printer has received a character and is ready to accept another. A 1 means that it is still reading the last character sent or data has not been received.

Bit 5: PE. This bit reflects the state of the 82C711/712 PE input pin. A 1 indicates a paper end condition. A 0 indicates the presence of paper.

Bit 4: SLCT. This bit reflects the state of the 82C711/712 SLCT input pin. A 1 means the printer is online. A 0 means it is not selected.

Bit 3: $\overline{\text{ERROR}}$ This bit reflects the inverted state of the 82C711/712 $\overline{\text{ERROR}}$ input pin. A 0 means that an error condition has been detected. A 1 indicates no errors.

Bits 2-0: Reserved.

3.2.3 *Printer Controls Register (Port C)*

Offset = 02H

This read/write register is located at an offset of 02H from the base address of the parallel port. Bit definitions are:

Bits 7-6: Reserved. Reset to 0.

Bit 5: Parallel Control Direction, valid in extended mode only (CR#1 <6>=1). In printer mode, the direction is always out, regardless of the state of this bit. In the extended mode, a 0 means an output/write condition. A 1 means an input/read condition.

Bit 4: IRQEN. This bit is used to enable or disable interrupts resulting from the printer $\overline{\text{ACK}}$ signal. A 1 generates interrupts when $\overline{\text{ACK}}$ changes from active to inactive. A 0 means that IRQ is disabled.

Bit 3: $\overline{\text{SLCTIN}}$ (pin 73, $\overline{\text{SLCTIN}}$). Used to drive the 82C711/712 $\overline{\text{SLCTIN}}$ output pin. A 1 selects the printer. A 0 means the printer is not selected.

Bit 2: $\overline{\text{INIT}}$ (pin 74, $\overline{\text{INIT}}$). Used to control the 82C711/712 $\overline{\text{INIT}}$ output pin. A 0 (active low) starts the printer (50 μs pulse minimum). A 0 initializes the printer.

Bit 1: $\overline{\text{AUTOFD}}$ (pin 76, $\overline{\text{AUTOFD}}$). Used to control the 82C711/712 $\overline{\text{AUTOFD}}$ output pin. A 1 causes the printer to generate a line feed after each line is printed. A 0 means no autofeed.

Bit 0: $\overline{\text{STROBE}}$ (pin 77, $\overline{\text{STROBE}}$). Used to control the 82C711/712 $\overline{\text{STROBE}}$ output pin. A 1 in this bit generates the active low pulse (0.5 μs pulse minimum) which is required to clock data into the printer. There is a 0.5 μs data setup time requirement before $\overline{\text{STROBE}}$ can be asserted. A 0 means there will be no strobe.

3.3 Parallel Port Connector

The parallel port connector is a DB-25 female connector. The 82C711/712 parallel port signals are connected directly to the parallel port connector. Typically the signals are assigned to the pins as shown below:

Pin	I/O	Name
1	O	$\overline{\text{STROBE}}$
2-9	I/O	PD0-PD7
10	I	$\overline{\text{ACK}}$
11	I	BUSY
12	I	PE
13	I	SLCT
14	O	$\overline{\text{AUTOFD}}$
15	I	$\overline{\text{ERROR}}$
16	O	$\overline{\text{INT}}$
17	O	$\overline{\text{SLCTIN}}$

Table 3.1 Summary of Accessible Parallel Port Registers

PORT		7	6	5	4	3	2	1	0
A	XX0H	DATA							
B	XX1H	BUSY	$\overline{\text{ACK}}$	PE	SCLTIN	$\overline{\text{ERROR}}$	R	R	R
C	XX2H	R	R	DIR	IRQEN	SLCTIN	$\overline{\text{INT}}$	AUTOFD	STROBE

Note: R means Reserved

(PORT A) DATA LATCH
(PORT B) STATUS
(PORT C) CONTROL

4.0 INTEGRATED DRIVE ELECTRONICS INTERFACE

4.1 Introduction

The IDE interface allows users to utilize hard disks with imbedded controller (AT and XT interface). The 82C711/712 provides the control signals for the IDE interface and the IDE buffers, as shown below:

IDEENLO:	Low Byte Buffer Enable (AT and XT).
IDEENHI:	High Byte Buffer Enable (AT only).
HDCS0:	Primary Hard Disk Chip Select used to access the Task File Registers decodes 1F0H-1F7H (AT) or 320H-323H (XT).
HDCS1:	Secondary Hard Disk Chip Select, decodes 3F6H-3F7H (AT and XT).
IOCS16:	When active it indicates 16 bit I/O transfer (AT only).
IDED7:	D7 of the IDE interface should be connected to this pin (AT only).
HDACK:	Hard Disk DMA Acknowledge (XT only).

IDEENLO becomes active when the 82C711/712 decodes addresses 1F0H-1F7H, 3F6H, and 3F7H in the AT mode, or 320H-323H and DMA transfers (HDACK=0) in the XT mode. IDEENHI becomes active only when IOCS16 is active and address range 1F0H-1F7H, and in AT mode (CR#00H<1>=1). IOCS16 is generated by the Hard Disk Controller when it requires a 16 bit transfer. IDED7 should be connected directly to data bit 7 of the IDE interface. The AT mode supports programmed I/O only (8 and 16 bit). XT mode supports only 8 bit DMA and 8 bit programmed I/O. The IOCS16/HDACK pin is multiplexed, in the AT mode it is IOCS16 in the XT mode it is HDACK signal.

4.2 AT/XT modes in IDE interface

There are 2 IDE interface modes:

AT mode: 8/16 bit programmed I/O only (no DMA). AT mode decodes addresses 1F0H-1F7H, 3F6H and 3F7H. Normal transfer is 8 bit; 16 bit transfer is performed when IOCS16 is active and on data register (1F0H). Both IDEENLO (low buffer enable) and IDEENHI (high buffer enable) are active during 16 bit transfer. HDCS0 is active whenever the 82C711/712 decodes programmed I/O address 1F0H-1F7H. IDEENLO is active on all AT mode addresses. On the low byte buffer, only 7 bits (D0-D6) are connected to the data bus. Bit 7 is a special case; it is sourced from the 82C711/712. On the IDE interface, IDED7 is connected directly to the connector. D7 of the 82C711/712 provides data bit 7 to the host interface. Normally the 82C711/712 functions as a buffer for D7, but, when reading 3F7H, D0-D6 of the 82C711/712 are tri-stated and IDEENLO is enabled to transfer data bits D0-D6 from the IDE to the host; D7 should be supplied by the Floppy Disk Interface.

XT mode: 8 bit programmed I/O or DMA (no 16 bit). Normally DMA transfer is done from the data register (320H) only. During a DMA cycle (indicated by active AEN and HDACK) IDEENLO is active, allowing the data to flow through the low byte buffer. XT mode decodes I/O address range 320H-323H. This is not available in the 82C712 (ADAPTER Application).

4.3 Hard Disk Register

Below is the short summary description and bit definition of the hard disk registers. More information can be obtained from IBM AT Technical Reference.

4.3.1 *Task File Registers*

Data Register (1F0H, R/W)

Read and Write to sector buffer. Accessed only when Read or Write command is executed.

Error Register (1F1H, R)

This register contains the status of the last executed command.

Bit 0:	Set 1 if Data Address Mark not found.
Bit 1:	Set 1 if track 0 is error.
Bit 2:	Set 1 if command is aborted.
Bit 3:	Not used.
Bit 4:	Set 1 if ID is not found.
Bit 5:	Not used.
Bit 6:	Set 1 if Data ECC error.
Bit 7:	Set 1 if bad block detect.

Write Compensation Register (1F1H, W)

This register contains the starting cylinder value divided by 4.

Sector Count Register (1F2H, R/W)

This register contains the number of sectors during a Verify, Read, Write or Format command. Note that a 0 value means 256 sector transfer.

Sector Number Register (1F3H, R/W)

This register contains the target's logical sector number of Read, Write and Verify command.

Cylinder Number Register (R/W)
1F4H = Low Byte, 1F5H = High Byte

These registers contain LSB and MSB of the first cylinder number where the disk is to be accessed for Read, Write, Seek and Verify command.

Drive/Head Register (1F6H, R/W)

Bit 7, 5:	Set to 1
Bit 6:	Set to 0
Bit 4:	Drive select. Primary = 0 Secondary = 1
Bit 3-0:	4 bit binary represents the head number (bit 3:MSB and bit 0:LSB)

Status Register (1F7H, R)

This register contains the status of the drive:

Bit 7:	Set to 1 if the drive is busy.
Bit 6:	Set to 1 if the drive is ready to accept command.
Bit 5:	Set to 1 if write fault condition occurred.
Bit 4:	Set to 1 if seek command is completed.
Bit 3:	Set to 1 if drive is ready to transfer data.
Bit 2:	Set to 1 if data correction is sucessful.
Bit 1:	Set to 1 if index mark is detected.
Bit 0:	Set to 1 if error occur from last command.

Command Register (1F7H, W)

This register contains command op code for fixed disk operation.

4.3.2 Other Registers

Digital Input Register Definition (3F7H, R)

Bit 7:	Diskette Change, Diskette interface status (FDC)
Bit 6:	Write Gate (HDC)
Bit 5:	Head Select 3/Reduced Write Current (HDC)
Bit 4:	Head Select 2 (HDC)
Bit 3:	Head Select 1 (HDC)
Bit 2:	Head Select 0 (HDC)
Bit 1:	Drive Select 1 (HDC)
Bit 0:	Drive Select 0 (HDC)

Fixed Disk Register (3F6H, W)

Bits 7-4: Not Used
Bit 3: HEAD3EN
Bit 2: RESET
0 = Normal operation, default
1 = Generate reset to HDC
Bit 1: $\overline{\text{IRQEN}}$
0 = Enabled interrupt
1 = Disable interrupt, default
Bit 0: Reserved

5.0 FLOPPY DISK CONTROLLER (FDC)

5.1 Introduction

The 82C711/712 contains a fully compatible NEC μPD72065B Floppy Disk Controller (FDC), an on-chip precision Analog Data Separator (ADS) and many other enhancement features. The XT/AT bus interface circuitry is completely integrated with the 82C711/712 and requires no external logic when interfaced with the XT/AT bus. The licensed 765 core guarantees the compatibility. The on-chip Data Separator supports 250/300/500Kb/s and 1Mb/s. Depending on the selected data rate, up to 3 external filters are automatically switched in. This provides optimum performance in the PC environment which uses 250/300 and 500Kb/s data rates. The 48 mA Floppy interface buffer allows the 82C711/712 to connect directly to the disk drive.

5.2 Floppy Disk Register Description

The 82C711/712 contains 5 registers which may be accessed by the main system processor. The description of each register is shown below:

Main Status Register (3F4H, Read only)

The Main Status Register contains the information for the FDC, and may be accessed any time.

Bit 7: Request for Master (RQM). This bit indicates that the data register is ready to send or receive data to or from the CPU. Both bits DIO and RQM should be used to perform the handshaking function of "ready" and "direction" to the CPU.

Bit 6: Data Direction (DIO). This bit indicates the direction of data transfer between the FDC and the data register. If DIO=1, then data is transferred from the data register to the CPU. If DIO=0, then transfer is from the CPU to the data register.

Bit 5: Execution Mode (EXM). This bit is set only when the execution phase is in the non DMA mode. When this bit goes low, the execution phase has ended and the result phase has begun. This bit operates only in the non DMA mode.

Bit 4: Command in progress. Set high when the Read or Write command is in progress. The FDC will not accept any other command.

Bit 3: Drive 3 seeking. Set high when drive 3 is in the Seek mode. The FDC will not accept any other command.

Bit 2: Drive 2 seeking. Set high when drive 2 is in the Seek mode. The FDC will not accept any other command.

Bit 1: Drive 1 seeking. Set high when drive 1 is in the Seek mode. The FDC will not accept any other command.

Bit 0: Drive 0 seeking. Set high when drive 0 is in the Seek mode. The FDC will not accept any other command.

Note: Some softwares write to this register instead of register 3F5H. For some NMOS 765 FDCs, a write to register 3F4H acts the same as a write to register 3F5H. For all CMOS 765s and the 82C711/712, a write to register 3F4H is ignored.

Data Register (3F5H, Read/Write)

All Commands, Status, and Data transferred between the CPU and the FDC flows through this register. The command is loaded into this register based on the Request for Master and Data Direction bits (bits 7 and 6 of Main Status Register).

During the Command phase, all information required to perform a particular operation is written into the Data Register.

During the Result phase, the Result Status is read from the Data Register (it actually consists of four status registers, ST0-ST3, in the stack with only one presented to the bus at a time).

Status Register 0 (ST0)

Bits 7-6: Interrupt Code (IC)

b7,	b6	
0	0	Normal termination of program completed.
0	1	Abnormal Termination of command. (AT)
1	0	Invalid Command issued.
1	1	Ready signal changed during execution.

Bit 5: Seek End (SE). Set high to indicate the completion of Seek command.

Bit 4: Equipment Check (EC). Set high to indicate track 0 signal failed or Fault signal received.

Bit 3: Not Ready (NR). Always set to 0.

Bit 2: Head Select (HS). Set high to indicate the state of head at interrupt.

Bit 1: Unit Select 1 (US1). This flag indicates a drive unit number at interrupt.

Bit 0: Unit Select 0 (US0). This flag indicates a drive unit number at interrupt.

Status Register 1 (ST1)

Bit 7: End of cylinder (EN). Set high to indicate that the FDC has tried to access a sector beyond the final sector of a cylinder.

Bit 6: Not used. Always set to 0.

Bit 5: Data Error (DE). Set high to indicate the FDC detects a CRC error in ID field or data field.

Bit 4: Overrun (OR). Set high to indicate the FDC is not serviced by the CPU during the data transfer within a certain time interval.

Bit 3: Not used. Always set to 0.

Bit 2: No Data (ND). Set high to indicate:

1) The FDC can not find the sector specified in Internal Data Register (IDR) during the execution of READ DATA, WRITE DELETED or SCAN command.

2) The FDC read ID field without an error during the execution of READ ID command.

3) The FDC cannot find the starting sector during the execution of READ A CYLINDER.

Bit 1: Not writable (NW). Set high to indicate the Write Protect signal is detected during execution of WRITE DATA, WRITE DELETED DATA, FORMAT A CYLINDER commands.

Bit 0: Missing Address Mark (MA). Set high to indicate that the FDC cannot detect Data Address Mark or Deleted Data Address Mark.

Status Register 2 (ST2)

Bit 7: Not used. Always set to 0.

Bit 6: Control Mark (CM). Set high to indicate the FDC encountered a sector which contains a Deleted Data Address Mark during the execution of READ DATA or SCAN command.

Bit 5: Data Error (DE). Set high to indicate the FDC detects a CRC error in the data field.

Bit 4: Wrong Cylinder (WC). Set high to indicate the content of the cylinder is different from that stored in the Internal Data Register (IDR).

Bit 3: Scan Equal Hit (SH). Set high to indicate the condition "equal" has been satisfied during the execution of SCAN command.

Bit 2: Scan Not Satisfied (SN). Set high to indicate the FDC cannot find a sector on the cylinder which meets the specified condition during the execution of SCAN command.

Bit 1: Bad cylinder (BC). Set high to indicate the content of the cylinder on the medium is different from that stored in IDR and the content of the cylinder is FFH.

Bit 0: Missing Address Mark (MD). Set high to indicate that the FDC can not find the Data Address Mark or Deleted Data Address Mark when reading the drive.

Status Register 3 (ST3)

Bit 7: Fault (F). Indicates the status of the Fault signal from the Floppy Disk Drive (FDD).

Bit 6: Write Protected (WP). Indicates the status of the Write Protected signal from the FDD.

Bit 5: Ready (RY). Indicates the status of the Ready signal from the FDD.

Bit 4: Track 0 Cylinder (T0). Indicates the status of the Track 0 signal from the FDD.

Bit 3: Two Side (TS). Indicates the status of the Two Side signal from the FDD.

Bit 2: Head Address (HD). Indicates the status of the Side Select signal to the FDD.

Bit 1: Unit Select 1 (US1). Indicates the status of the Unit Select 1 signal to the FDD.

Bit 0: Unit Select 0 (US0). Indicates the status of the Unit Select 0 signal to the FDD.

NOTE: μPD765 internal drive select bits US0 and US1 are not used.

Digital Output Register (Drive Control Register) (3F2H Write only)

This 8-bit write only register controls the drive select, motor enable, DMA enable and reset functions.

Bit 7: Motor Enable 3.
Bit 6: Motor Enable 2.
Bit 5: Motor Enable 1.
Bit 4: Motor Enable 0.
Bit 3: Enable DMA (DRQ and $\overline{\text{DACK}}$) and interrupt (IRQ).
Bit 2: Reset floppy controller.
Bits 1,0: Drive selects.

Below is the Drive/Motor activation table.

Table 5.1 Drive/Motor Selection

b7	b6	b5	b4	b1	b0	Driver
			1	0	0	0
		1		0	1	1
	1			1	0	2
1				1	1	3

Configuration Control Register (Data Rate Register) (3F7H Write only)

This is a two bit register that controls the data rate the controller uses. This register feeds the logic that selects the data rates by programming a prescaler that divides the crystal or clock input by either 3, 5, or 6. This causes either 4 MHz, 4.8 MHz or 8 MHz to be input as the master clock for the controller core.

Bit 7-2: Not used.

Bits 1, 0: Data Rate select (determined as shown in Table 5.8 in the PLL filter section).

Fixed Disk Register (3F7H, Read only)

Bit 7: Disk changed. This bit is the complement of the Disk Changed input pin.

Bits 6-0: These bits are used by the Hard Disk Controller. They are tri-stated when reading this register.

5.3 Command Sequence

The 82C711/712 FDC is capable of generating 17 different commands. Each command is initiated by a multi-byte transfer from the CPU, and the result after execution may also be multi-byte transferred back to the CPU. Most commands involve three phases:

COMMAND PHASE: The FDC receives all information required to perform a particular operation.

EXECUTION PHASE: The FDC performs the instructed command.

RESULT PHASE: After completion of the operation, status and other housekeeping information is made available to the CPU.

5.4 Modes of Operation

DMA Mode

If the DMA mode is selected, a DMA request is initiated in the Execution phase when a byte is ready to be transferred. The DMA mode is enabled via the DMA bit in the SPECIFY command, and the DMA signals are enabled via the Drive Control Register. After the last byte is transferred, an interrupt is generated to indicate the beginning of the Result phase.

Interrupt Mode (Non-DMA)

If Non-DMA is selected, an interrupt is generated in the Execution phase when a byte is ready to be transferred. The Main status register is read to verify that the interrupt is for data transfer. When data is read or written to the Data Register, the interrupt will be cleared. When the last byte is transferred, the interrupt is also generated to indicate the beginning of Result phase.

5.5 Command Description

Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation". The Read Data Command may be terminated by the receipt of a Terminal Count (TC) signal. TC should be issued at the same time that the $\overline{\text{DACK}}$ for the last byte to data is sent. Upon receipt of this

signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 5.2 below shows the Transfer Capacity.

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completed at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, the DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexadecimal.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

Table 5.2 Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, then the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 microsec in the FM Mode, and every 13 microsec in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 5.3 shows the value for C, H, R, and N, when the processor terminates the Command.

Write Data

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the Specify Command), and begins reading ID Fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 09 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N $\neq$ 0.

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 microsec in the FM mode, and every 13 microsec in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively).

Write Deleted Data

The command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

Table 5.3

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
0	0	Equal to EOT	C + 1	NC	R = 01	NC
0	1	Less than EOT	NC	NC	R + 1	NC
0	1	Equal to EOT	C + 1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
1	0	Equal to EOT	NC	LSB	R = 01	NC
1	1	Less than EOT	NC	NC	R + 1	NC
1	1	Equal to EOT	C + 1	LSB	R = 01	NC

Notes:
1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Read Deleted Data

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field and SK = 09 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

Read a Track

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command. This command terminates when number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, it sets the MA (missing address mark) flag in Status register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

Read ID

The READ ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format a Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3470 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (Number of bytes/sector), SC (Sectors/Cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with non sequential sector numbers, if desired.

The processor must now send new values for C, H, R, and N to the FDC for each sector on the track. If FDC is set for DMA mode, it will issue four DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively. Table 5.4 shows the relationship between N, SC, and GPL for various sector sizes.

Scan Commands

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{PROCESSOR}$, $D_{FDD} < D_{PROCESSOR}$, or $D_{FDD} > D_{PROCESSOR}$. The hexadecimal byte of FF either from memory or FDD can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented ($R + STP \rightarrow R$), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 5.5 shows the status of bits SH and SN under various conditions of Scan.

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

Table 5.4

Mode	Sector Size	N	SC	GPL(1)	GPL(2,3)
	8" Drives (360 RPM, 500 Kb/s)				
FM	128	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM(4)	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
	5 1/4" DRIVES (300 RPM, 250 KB/S)				
FM	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM(4)	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
	3 1/2" DRIVES (300 RPM, 250 KB/S)				
FM	128	00	0F	07	1B
	256	01	09	0E	2A
	512	02	05	1B	3A
MFM (4)	256	01	0F	0E	36
	512	02	09	1B	54
	1024	03	05	35	74

Notes:
1. Suggested values of GPL in Read or Write command to avoid splice point between data field and ID field of contiguous sections.
2. Suggested value of GPL in Format command.
3. All values except sector size are hexidecimal.
4. In MFM mode the FDC cannot perform a Read/Write/Format operation with 128 bytes/sector (N=00).

Table 5.5 Scan Conditions

Command	Status Register 2 Bit2 = SN	Status Register 2 Bit3 = SH	Comment
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and the Scan Command is started at sector 21, the following will happen: sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT has been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 microsec (FM Mode) or 13 microsec (MFM Mode). If an Overrun occurs, the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number) and, if there is a difference, performs the following operation:

PCN < NCN: Direction signal of FDD set to a 1 (high), and Step Pulses are issued. (Step In.)
PCN > NCN: Direction signal of FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits DB_0 - DB_3 in Main Status Register are set during seek operation and are cleared by Sense Interrupt Status command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON-BUSY state. While the FDC is in the NON-BUSY state, another Seek Command may be issued, and in this manner parallel seek operation may

be done on up to 4 Drives at once. No other command could be issued for as long as FDC is in the process of sending Step Pulses to any drive.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write three bytes of Seek command exceeds 150 microsec, the timing between first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

Recalibrate

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs) and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the Seek Command, also applies to the RECALIBRATE Command. If the diskette has more than 77 tracks, the RECALIBRATE command should be issued twice, in order to position the read/write head to the Track 0.

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in NON-DMA Mode, DB_5 in Main Status Register is high. Upon entering Result Phase this bit gets cleared. Reason 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by reading/writing data to FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command, when issued, resets the interrupt signal and, via bits 5,6, and 7 of Status Register 0, identifies the cause of the interrupt. See Table 5.6.

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to issue a Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

Issuing Sense Interrupt Status Command without interrupt pending is treated as an invalid command.

Specify

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the

Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms ... 0F = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms, ... 7F = 254 ms).

The time intervals mentioned above are a direct function of the clock. Times indicated above are for an 8 MHz clock; if the clock was reduced to 4 MHz (mini-floppy application), then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

Invalid

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the FDC765 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high (1), indicating to the processor that the FDC is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0 it will find an 80 hex indicating an Invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

Version

The Version command was added to distinguish the μPD765B from the μPD765A. The response to this command is the same as the Invalid command except that a processor read of Status Register 0 returns 90 Hex instead of 80 Hex.

5.6 Analog Data Separator

The 82C711/712 on-chip Analog Data Separator (ADS) consists of an analog Phase Lock Loop (PLL) and its associated circuitry. The PLL is composed of four main components: the phase comparator, filter, Voltage Control Oscillator (VCO) and programmable divider. The phase comparator detects the phase difference between the raw data read from the disk and the divider's output. The phase difference is converted to a current which either charges or discharges the filter. This reduces the phase

Table 5.6 Interrupt Status

STATUS REGISTER 0			
SEEK END	INTERRUPT CODE		
BITS 5	BIT 6	BIT 7	CAUSE
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

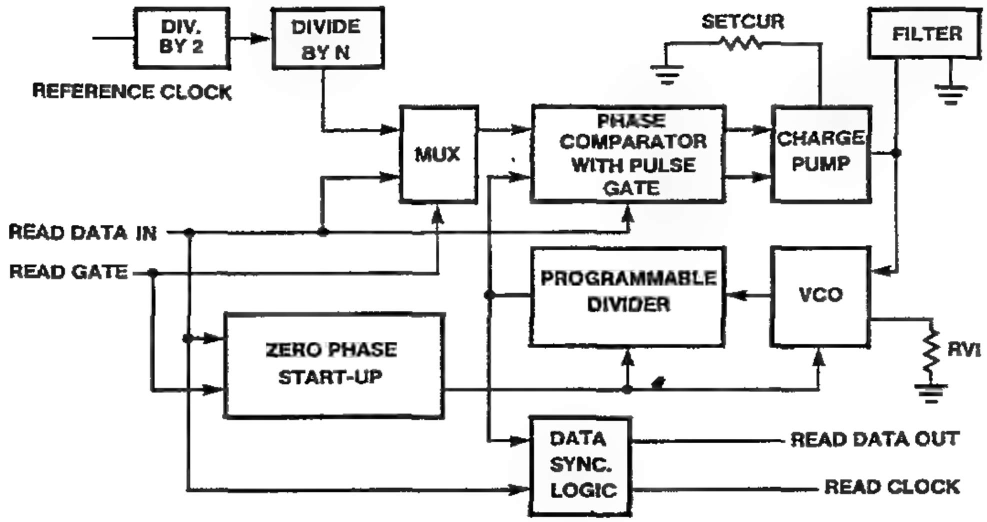


Figure 5.1 Analog Data Separator Block Diagram

difference until the divider output frequency matches the average frequency of the data read from the disk. The block diagram of the Data Separator is shown in Figure 5.1.

PLL Filter

The 82C711/712 Analog Data Separator requires an external filter in order to run at different data rates. This filter functions as the current sink and source when the phase difference is converted to a current. Figure 5.2 is a typical 250/300/500 Kb/s and 1 Mb/S filter configuration with recommended values (Table 5.7).

Table 5.7: Filter Values

R1	R2	R3	C1	C2	C3	C4
1.2K ±5%	18.2K ±1%	6.81K ±1%	1500 pF	0.027 μF	0.0047 μF	0.0047 μF

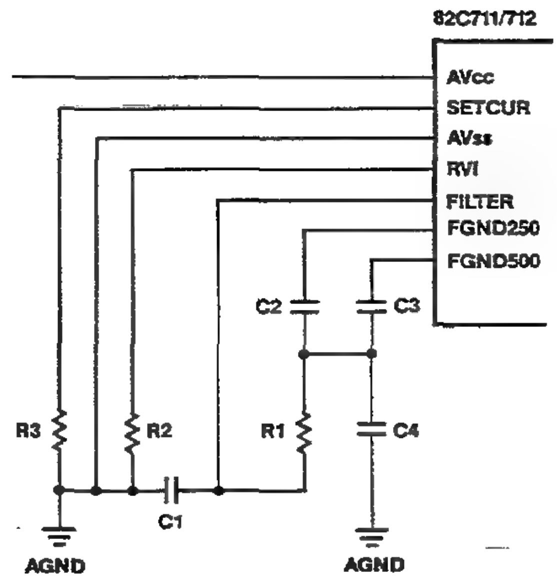


Figure 5.2 Filter Configuration

5.7 Drive Polling

After the reset has been sent to the 82C711/712, the FDC will automatically go into the polling mode. In between commands, the FDC polls all the drives looking for a change in ready line from any of the drives. If the ready line changes state (usually due to a door opening or closing), then the FDC will generate an interrupt. When the status register 0 (ST0) is read (after the Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the ready line by the FDC occurs continuously between commands, thus notifying the CPU which drives are on and off line. Each drive is polled every 1.024ms except during Read/Write command. When using the 4MHz clock for interfacing mini floppies, the polling is 2.048ms.

5.8 Crystal/Clock

The 24 MHz crystal clock can be supplied by either crystal or MOS level oscillator. The typical crystal circuit with recommended values is shown in Figure 5.3.

Typical values for C1 and C2 are 20pF.

Crystal Specification:

Frequency:	24MHz
Mode:	Series Resonant Fundamental Mode
Shunt capacitance:	Less than 7pF
Maximum ESR:	35 Ohms

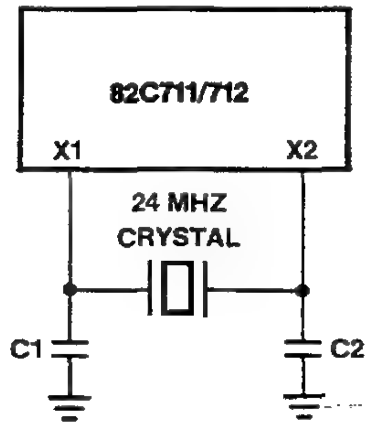


Figure 5.3 Crystal Circuit

Table 5.8: Data Rate and Precompensation Programming Values

D1 D0 **	DRVTYP Pin	Data Rate MFM (Kb/s)	Normal Precomp* (ns)	Alternate Precomp* (ns)	FGND pin Enabled	RPM/LC Pin Level
0 0	X	500	125	125	FGND500	High
0 1	0	250	125	250	FGND250	Low
0 1	1	300	208	208	FGND250	Low
1 0	0	250	125	250	FGND250	Low
1 0	1	250	125	250	FGND250	Low
1 1	0	1000	63	83	None	High
1 1	1	1000	83	83	None	Low

* Normal values when PUMP/PREN pin set low; Alternate values when PUMP/PREN pin set high.
** D0 and D1 are Data Rate Control Bits.

5.9 Instruction Set Table

The following pages are Command symbol description and μP756 instruction sets.

Table 5.9: Instruction Set Table

SYMBOL DESCRIPTION

SYMBOL	NAME	DESCRIPTION
C	Cylinder Number	The current/selected cylinder (track) numbers 0 through 76 of the medium.
D	Data	The Data pattern which is going to be written into a Sector.
D7-D0	Data Bus	8-Bit Data bus. D7 is a most significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the Data Length which users are going to read out or write into the Sector.
EOT	End Of Track	The final Sector number of the Cylinder. During R/W, the FDC stops data transfer after a sector number equal to EOT.
GPL	Gap Length	The length of Gap 3. During R/W command, this value determines the number of bytes that VCO sync will stay low after two CRC bytes. During Format, it determines the size of Gap 3.
H	Head Address	Head Number 0 or 1 as specified in ID field.
HD	Head	Selected head number 0 or 1. (H = HD in all command words).
HLT	Head Load Time	Head Load Time in the FDD (2 to 254 ms in 2ms steps).
HUT	Head Unload Time	Head Unload time after Read/Write operation (16 to 240ms in 16ms increments).
MF	FM or MFM mode	If MF is low, FM mode is selected. High selects MFM mode.
MT	Multi-Track	If MT is high, multi-track operation is performed. If MT = 1 after finishing the R/W on side 0, FDC automatically starts searching for sector 1 on side 1.
N	Number	Number of Data Bytes written into a sector.
NCN	New Cylinder Num.	New Cylinder Number which is going to be reached as a result of the Seek operation; Desired position of Head.
ND	Non-DMA mode	Operation in non-DMA mode.
PCN	Present Cyl. Num.	Cylinder number at the completion of SENSE INTERRUPT Status command, Position of Head at the present time.
R	Record	Sector number which will be read or written.
R/W	Read/Write	Read or Write signal.
SC	Sector	Number of Sectors per Cylinder.
SK	Skip	Skip Deleted Data Address Mark.
SRT	Step Rate Time	Stepping rate of FDD. (1 to 16ms in 1ms increments.) Stepping rate applies to all drives (FH = 1ms, EH = 2ms)

Table 5.9: **Instruction Set Table** (Continued)

SYMBOL	NAME	DESCRIPTION
ST0-ST3	Status 0-3	Four registers store the status information after a command is executed. This information is available during the result phase and read only after a command has been executed.
STP		During SCAN operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the CPU; and if STP = 2, the alternate sectors are read and compared.
US0, US1	Unit Select	Selected drive number 0 or 1. Programmed in commands. Not used for external drive selection, which is based on Digital Output Register.

82C711/712 Instruction Set

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		Data Bus								
Format A Track										
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	(Note)
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filter Byte
Execution										FDC formats entire track
Result	R	ST 0								Status Information after Command Execution
	R	ST 1								
	R	ST 2								
	R	C								ID information has no meaning
	R	H								
	R	R								
	R	N								
Recalibrate										
Command	W	0	0	0	0	0	1	1	1	Command Codes
Execution	W	X	X	X	X	X	0	US1	US0	Head retracted to Track 0

82C711/712 Instruction Set (Continued)

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Seek										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	NCN								
Execution										Head is positioned over proper cylinder on diskette.
Invalid										
Command	W	*Invalid Codes*								Invalid Codes FDC in standby
Result	R	ST 0								ST 0 = 80H
Read ID										
Command	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on cylinder is stored in Data Register
Result	R	ST 0								Status information after command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID read during execution phase from floppy disk
	R	H								
	R	R								
	R	N								
Sense Interrupt Status										
	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information at the end of Seek operation about FDC
	R	PCN								

82C711/712 Instruction Set (Continued)

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
					Data Bus					
Sense Drive Interrupt										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	R					ST 3				Status information about the FDD
Specify										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	
Version										
Command	W	X	X	X	1	0	0	0	0	Invalid Code FDD in standby
Result	R					ST 0				ST 0 = 90H
Read A Track										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID information prior to Command execution.
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between the FDD and main system. FDC reads all data fields fro index hole to EOT
Result	R					ST 0				Status information after command execution
	R					ST 1				
	R					ST 2				
	R					C				Sector ID information after command execution
	R					H				
	R					R				
	R					N				

82C711/712 Instruction Set (Continued)

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		Data Bus								
Scan Low or Equal										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID information prior to Command execution.
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data compared between the FDD and main system
Result	R					ST 0				Status information after command execution
	R					ST 1				
	R					ST 2				
	R					C				Sector ID information after command execution
	R					H				
	R					R				
	R					N				
Scan Equal										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID information prior to Command execution.
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data compared between FDD and main system
Result	R					ST 0				Status information after command execution
	R					ST 1				
	R					ST 2				
	R					C				Sector ID information after command execution
	R					H				
	R					R				
	R					N				

82C711/712 Instruction Set (Continued)

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
		Data Bus								
Scan High or Equal										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID
	W					H				information prior
	W					R				to Command
	W					N				execution.
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data compared between FDD and main system
Result	R					ST 0				Status
	R					ST 1				information after
	R					ST 2				command execution
	R					C				Sector ID
	R					H				information after
	R					R				command
	R					N				execution
Read Data										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID
	W					H				information prior
	W					R				to Command
	W					N				execution. The 4
	W					EOT				bytes are
	W					GPL				commanded
	W					DTL				against header on floppy disk.
Execution										Data transfer between CPU and FDD
Result	R					ST 0				Status
	R					ST 1				information after
	R					ST 2				command execution
	R					C				Sector ID
	R					H				information after
	R					R				command
	R					N				execution

82C711/712 Instruction Set (Continued)

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Write Data										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID information prior to Command execution. The 4 bytes are commanded against header on floppy disk.
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between CPU and FDD
Result	R					ST 0				Status information after command execution
	R					ST 1				
	R					ST 2				
	R					C				Sector ID information after command execution
	R					H				
	R					R				
	R					N				
Read Deleted Data										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID information prior to Command execution. The 4 bytes are commanded against header.
	W					H				
	W					R				
	W					N				
	W					EOT				
	W					GPL				
	W					DTL				
Execution										Data transfer between CPU and FDD
Result	R					ST 0				Status information after command execution
	R					ST 1				
	R					ST 2				
	R					C				Sector ID information after command execution
	R					H				
	R					R				
	R					N				

82C711/712 Instruction Set (Continued)

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Write Deleted Data										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W					C				Sector ID
	W					H				information prior
	W					R				to Command
	W					N				execution. The 4
	W					EOT				bytes are
	W					GPL				commanded
	W					DTL				against header.
Execution										Data transfer between CPU and FDD
Result	R					ST 0				Status
	R					ST 1				information after
	R					ST 2				command execution
	R					C				Sector ID
	R					H				information after
	R					R				command
	R					N				execution

Note:X = Don't care, usually made to equal 0.

6.0 THE 82C711/712 CONFIGURATION

6.1 Introduction

The 82C711 is configured by software and the 82C712 is configured by hardware.

In MOTHERBOARD (82C711) mode (the 82C711 is embedded in motherboard), all configuration is programmed via software, to be user-friendly (probably menu-driven). The 82C711 configuration portion can be built into the existing BIOS or the 82C711 setup utilities is provided with system. DIP switches and jumpers can thus be eliminated meaning that it should no longer be necessary to open the chassis to change the configuration of a peripheral

In ADAPTER (82C712) mode, configuration is done via hardware (jumper select). This allows the 82C712 to eliminate an expensive configuration ROM. Two serial ports, parallel port (IBM PC/AT printer mode), IDE AT and FDC are available in this mode. Also, IRQ is active high only.

6.2 82C711 Configuration (MOTHERBOARD Application)

In order to setup or change the configuration of the UPC, two consecutive I/O addresses (one even and one odd; these should not conflict with any existing devices) are used to select and access the internal configuration registers. The configuration sequence is intentionally complicated to prevent accidental changes to the UPC configuration by an errant program. Any deviation from the sequence described below will cause the configuration state machine to return to its initial idle state.

By IBM PC convention, the addresses 3F0H-3F7H are reserved for Floppy Disk Controller (FDC). In the 82C711, 3F0H-3F1H addresses are used for configuration of the state machine.

The configuration sequence is divided into three steps:

1) Entering the configuration mode
2) Configuring the 82C711
3) Escaping the configuration mode.

The description of each step with examples is as follows:

6.2.1 *Entering configuration mode*

To enter the configuration mode, write two consecutive 55H to port 3F0H. Note that any deviation from the above sequence will cause the configuration state machine to return to its initial idle state.

Example: (In 80XX assembly language):

```
MOV    DX,3F0H    ;Port Address
MOV    AL,55H     ;Data
OUT    DX,AL
OUT    DX,AL
```

********* In Configuration Mode *********

6.2.2 *Configuring the 82C711*

The 82C711 has four configuration registers (CR0-CR3) which can be written to or read.

To write data to CR0-CR3

—Write XNH to 3F0H where
N = 0 to 3 (Bit 0-3 are used).
(Configuration Index Register)
X = 4 to 7 (Bit 4-7 are don't care)

—Write <data> to 3F1H where
<data> = data needed to be written into register pointed by the Index Register.

To read the content from the CR0-CR3, the bit 7 of CR#1 needs to be set to 1 to enable the reading of these registers.

—Write XNH to 3F0H where
N = 0 to 3 (Bit 0-3 are used).
(Configuration Index Register)
X = 4 to 7 (Bit 4-7 are don't care)

—Read <data> from 3F1H

Examples:

To access register 0 to turn on the oscillator and enable all ports:

```
MOV     DX,3F0H     ;Access CR#0
MOV     AL,00H
OUT     DX,AL
MOV     DX,3F1H     ;Set necessary
MOV     AL,0BFH     ;bit
OUT     DX,AL
```

To access register 2 to set the serial port 1 address to Com 1, serial 2 in COM3 and put them in Normal mode.

```
MOV     DX,3F0H     ;Access CR#2
MOV     AL,02H
OUT     DX,AL
MOV     DX,3F1H
MOV     AL,0EAH
OUT     DX,AL
```

6.2.3 *Escaping configuration mode*

To escape configuration mode, write AAH value in port 3F0H

```
MOV     DX,3F0H
MOV     AL,0AAH
OUT     DX,AL
```

******* Out of Configuration Mode *******

6.2.4 *Configuration example*

The sample configuration program below is written in the 8086 assembly language.

```
************************************
       Enter configuration mode
************************************

MOV     DX,3F0H     ;Port Address
MOV     AX,55H      ;Data
OUT     DX,AL
OUT     DX,AL

************************************
         Configure the 82C711
************************************

MOV     DX,3F0H     ;Access CR#0
MOV     AL,00H
OUT     DX,AL
MOV     DX,3F1H     ;Set necessary
MOV     AL,0BFH     ;bit
OUT     DX,AL

MOV     DX,3F0H     ;Access CR#2
MOV     AL,02H
OUT     DX,AL
MOV     DX,3F1H
MOV     AL,0EAH
OUT     DX,AL

************************************
     Escape the configuration mode
************************************

MOV     DX,3F0H
MOV     AL,0AAH
OUT     DX,AL
```

6.3 Configuration Register Description (82C711 (MOTHERBOARD Application) ONLY)

There are 4 configuration registers in the 82C711 which must be initialized. Settings are retained as long as standby power is maintained.

These registers are not affected by the RESET signal and are set to their default state only upon power up. Table 6-1 depicts the configuration registers in the 82C711 with the default values upon power up. The definitions for each of the bits in the 82C711 configuration registers are shown below.

Configuration Register 00H

This register is located at CRI off-set 00H. Bit definitions are as follows:

Bit 7: Valid Configuration. This bit indicates that a valid configuration cycle has taken place. The configuration software should set this bit to 1 after it has initialized the required configuration registers.

Value	Function
0	Invalid Configuration. Indicates that power has been applied to the UPC but the configuration registers have not yet been fully initialized. A reset from the RESET pin has no effect on this bit. (Default upon power-up)
1	Valid Configuration. Indicates that the configuration software has initialized all necessary configuration registers since the last time power was applied to the UPC.

Bits 6-5: Serial Port and Floppy Oscillator Enable.

Value		Function
b6	b5	
0	0	Oscillator always ON
0	1	Oscillator is ON, BR Generator is ON when PWRGD is active, otherwise it is OFF, default.
1	0	Oscillator is ON, BR Generator is ON when PWRGD is active, otherwise it is OFF.
1	1	Oscillator always OFF

Value	Function
0	Oscillator ON, BR Generator Clock ENABLED. In this state the oscillator and Baud Rate Generator Clock are always enabled and are not shut off when the PWRGD pin becomes inactive.
1	Oscillator ON, BR Generator Clock ENABLED. In this state, the oscillator and BR Generator Clock are ON and ENABLED respectively as long as the PWRGD pin is active. When PWRGD becomes inactive, these two are shut down.
2	Oscillator ON, BR Generator Clock ENABLED. In this state, the oscillator and BR Generator Clock are ON and ENABLED respectively as long as the PWRGD pin is active. When PWRGD becomes inactive, these two are shut down.
3	Oscillator OFF, BR Generator Clock DISABLED.

Bit 4: Enable FDC.
0 FDC Disabled
1 FDC Enabled (Default)

Bit 3: Power up FDC.
0 FDC power down
1 FDC power up (default)

Bit 2: Reserved (R/W)

Bit 1: IDE AT/XT Select
0 IDE XT type
1 IDE AT type (Default)

Bit 0: Enable IDE
0 IDE Disabled
1 IDE Enabled (Default)

Configuration Register 01H

This register is located at CRI offset 01H. Bit definitions are as follows:

Bit 7: Enable CR0-CR3 reading bit
0 Disable the reading of CR0-CR3
1 Enable the reading of CR0-CR3 (default)

Bit 6,5: Select COM3,COM4 address

		COM3	COM4	
0	0	338H	238H	(Default)
0	1	3E8H	2E8H	
1	0	2E8H	2E0H	
1	1	220H	228H	

Bit 4: IRQ polarity select
0 IRQ active low, inactive is hi-Z
1 IRQ active high, inactive low (Default)

Note that when IRQ is active high, IRQ output is low when it is inactive. When IRQ is active low, IRQ output is tristated. This allows interrupt sharing.

Bit 3: Parallel port mode
0 Extended Parallel Port Mode (Bidirection)
1 Printer Mode (Default)

Bit 2: Parallel port power down
0 Power down mode
1 Normal mode (Default)

Bit 1,0: Parallel port Address selection

0	0	Disabled
0	1	3BCH
1	0	378H
1	1	278H (Default)

Configuration Register 02H

This register is located at CRI offset 02H. Bit definitions are as follows:

Bit 7: Secondary serial port power down
0 Power down mode
1 Normal mode (Default)

Bit 6: Secondary serial port disable
0 Disabled
1 Enabled (Default)

Bit 5,4: Secondary serial port address select

0	0	COM1,3F8H
0	1	COM2,2F8H (Default)
1	0	COM3, depending on bit 5,6 of CR#1
1	1	COM4, depending on bit 5,6 of CR#1

Bit 3: Primary serial port power down
0 Power down mode
1 Normal mode (Default)

Bit 2: Primary serial port disable
0 Disabled
1 Enabled (Default)

Bit 1,0: Primary serial port address select

0	0	COM1,3F8H (Default)
0	1	COM2,2F8H
1	0	COM3, depending on bit 5,6 of CR#1
1	1	COM4, depending on bit 5,6 of CR#1

Configuration Register 03H (Test only)

Bit 7: Secondary serial port test
0 Normal mode (Default)
1 Test mode

Bit 6: Primary serial port test
0 Normal mode (Default)
1 Test mode

Bit 5,4:

Value		Function
0	0	Normal mode. Test disable
0	1	TBD
1	0	TBD
1	1	TBD

Bits 3-0: TBD

6.4 82C712 (ADAPTER Application only) Hardware Configuration

The port addresses and enabling/disabling are determined by the jumper selects.

6.4.1 *Parallel Port Address Select*

PCF1	PCF0		
0	0	Disabled	
0	1	LPTA	3BCH
1	0	LPTB	378H
1	1	LPTC	278H

The parallel port supports the standard IBM printer port only.

6.4.2 *Serial Port Address Select*

Primary serial port

S1CF1	S1CF0		
0	0	Disabled	
0	1	COM3	338H
1	0	COM2	2F8H
1	1	COM1	3F8H

Secondary serial port

S2CF1	S2CF0		
0	0	Disabled	
0	1	COM4	238H
1	0	COM1	3F8H
1	1	COM2	2F8H

6.4.3 *IDE Control*

IDECF	
0	IDE Disabled
1	IDE Enabled

The IDE supports the AT type only.

6.4.4 *FDC Control*

FDCCF	
0	FDC Disabled
1	FDC Enabled

7.0 82C711 POWER MANAGEMENT

7.1 Introduction

The power management functions can be implemented in the MOTHERBOARD (82C711) mode only. Power management functions are achieved using PWRGD pin (hardware) and Configuration Register bits (software). The 82C711 configuration and register data can be retained during sleep mode with minimum current drain. This makes the 82C711 ideal for laptop environments. Each port of the 82C711 can also be disabled or powered down through configuration registers. This feature enhances the 82C711's flexibility in system integration. The section below discusses the power management of the 82C711.

7.2 Power Management Application

There are three typical operating modes for any system.

1) Active mode
2) Sleep mode
3) Power Down mode.

Table 6-1. The 82C711/712 Bit Definition Summary with Default Values

OFFSET	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	DEFAULT
00H	Valid	Osc Select		FDC Enable	FDC Pwrdwn	Resr	IDE AT/XT	IDE Enable	3FH
01H	Enable RConF	COM3,4 address		IRQ Polarity	Parallel Mode	Parallel Pwrdwn	Parallel address sel.		9FH
02H	UART2 Pwrdwn	UART2 Enable	UART2 address select		UART1 Pwrdwn	UART1 Enable	UART1 address select		DCH
03H	UART2 test	UART1 test	FDC Test select		Resvr. *	Resvr. *	Reserved *		00H

*TBD

Active mode:

In this mode, the 82C711 will be powered by a power supply (through AC outlet) or in a laptop by a main battery (NiCd). The configuration registers will be initialized by the System BIOS. In Active mode, software (BIOS) can power off selected resources when needed to reduce total power consumption.

Sleep mode:

In a Laptop application, the power source is the main battery which can last from 4-12 hours. To save battery energy, the system should be put in sleep mode which draws minimum current. The 82C711 supports this sleep mode feature through PWRGD pin and bits 6 and 5 of configuration register 0H (CR#0H<6,5>). Below is a detailed descrip tion of these bit functions.

b6,b5:	Serial Port & Floppy Oscillator Enable.
0 0	Oscillator always ON regardless of PWRGD.(default)
0 1	Oscillator is ON when PWRGD is high, otherwise it is OFF, (tri-state)
1 0	Oscillator is ON when PWRGD is high, otherwise it is OFF.(tri-state),
1 1	Oscillator is always OFF.

To implement the sleep mode, the CR#0H<6,5> should be programmed as 0,1 or 1,0. This turns off the oscillator and minimizes the current drawn by the serial and floppy ports. The PWRGD signal is controlled by user designed sleep mode circuitry. When the system is put in the sleep mode, the sleep mode circuitry will deassert PWRGD. The 82C711 isolates itself from the rest of the system; all outputs are tri-stated, all inputs are disabled and all commands are ignored until the PWRGD is restored to the active state (wake up). This is why CRD is set to 0, 1 or 1, 0.

Power Down mode

In this mode, the power is completely removed. from the system. The programmed configuration register data will not be retained. This should not be the issue since the configuration registers will be restored by the system BIOS.

Note: In any mode, the 82C711/712 should not be powered by the RTC backup battery (Lithium).

7.3 Enabled and Power Down Register Values

This section summarizes the Enabled/Disabled and Power Up/Down bits for each port.

Serial Port 1

CR#02H<2> = 1	Enabled (default)
CR#02H<2> = 0	Disabled
CR#02H<3> = 1	Power Up (default)
CR#02H<3> = 0	Power Down

Serial Port 2

CR#02H<6> = 1	Enabled (default)
CR#02H<6> = 0	Disabled
CR#02H<7> = 1	Power Up (default)
CR#02H<7> = 0	Power Down

Parallel Port

CR#01H<1,0> = 0,1 or 1,0 or 1,1	Enabled (Default)
CR#01H<1,0> = 0,0	Disabled
CR#01H<2> = 1	Power Up (default)
CR#01H<2> = 0	Power Down

Floppy Port

CR#00H<4> = 0	Disabled
CR#00H<4> = 1	Enabled (default)
CR#00H<3> = 1	Power Up (default)
CR#00H<3> = 0	Power Down

IDE port

CR#00H<0> = 0	Disabled
CR#00H<0> = 1	Enabled (default)

8.0 PC/AT DESIGN APPLICATION

8.1 Introduction

This section describes the 82C711/712 in a PC/AT application. With the 82C711, the complete 2 serial ports, parallel port, floppy disk port and IDE interface can be embedded in the motherboard with minimal board space and some cost saving. Figure 8.1 shows a typical motherboard application of the 82C711. Figure 8.2 shows a typical ADAPTER (82C712) mode application.

8.2 I/O Address Map for the PC/AT

Serial Port

Below is a table of standard PC/AT serial port addresses and the corresponding interrupts.

Physical Address	Interrupt	Logical Name
3F8H	IRQ4	COM1
2F8H	IRQ3	COM2
338H/3E8H 2E8H/220H	IRQ4	COM3
238H/2E8H 2E0H/228H	IRQ3	COM4

Note that the logical name has no bearing on the address assignment. For instance, COM1 logical name is assigned to the first serial port found by the ROM BIOS, regardless of the IRQ and address assignment. However, the address is paired with the assigned interrupt. Also, there is a sequence of the addresses the BIOS will search for.

By default, the 82C711/712 serial port is set at the 3F8H address, and the interrupt should be hard wired to the IRQ4.

Parallel Port

Physical Address	Interrupt	Logical Name
3BCH	IRQ5	LPTA
378H	IRQ7	LPTB
278H	IRQ5	LPTC

Note that the logical name has no bearing on the address assignment. For instance, LPT1 logical name is assigned to the first serial port found by the ROM BIOS, regardless of the IRQ and address assignment. However, the address is paired with the assigned interrupt. Also, there is a sequence of the addresses the BIOS will search for.

The IBM PC/AT allows installation of up to 3 parallel ports. These ports have logical names: LPT1, LPT2, LPT3. The printer port on the Monochrome/Printer Adaptor, which is addressed at 3BCH, will be LPT1 when it is installed, then the LPTC (278H) on 82C711 (if configured) will be LPT2.

By default, the 82C711/712 serial port is set at 278H address, and the interrupt should be hard wired to the IRQ5.

Floppy Disk Controller

The 82C711/712 integrates an entire PC/AT floppy controller design. The I/O address is mapped into 3F0H-3F7H; there is no need for an external address decoder. The 82C711/712 is connected directly to the floppy disk interface because of the on-chip 48 mA output buffer. The open collector outputs from the floppy disk interface should be terminated at the 82C711/712 with 150 ohm or 1K resistors. The external 250/300/500 Kb/s PLL filter is connected to the 82C711/712 via FILTER, FGND250, FGND500 and AGND pins. This filter configuration allows the 82C711/712 to operate at different data rates. The floppy interrupt is connected to IRQ6 as PC/AT standard. Below is the table of I/O address maps and drive/media formats.

I/O Address Map for Floppy

I/O Address	Access Type	Description
3F0H	—	Unused
3F1H	—	Unused
3F2H	Write	Digital Output Register
3F3H	—	Unused
3F4H	Read	Main Status Reg.
3F5H	R/W	Data Register
3F6H	—	Unused
3F7H	Write	Data Rate Select Reg.
3F7H	Read	Digital Input Register

The description of these registers can be found in the Floppy Section.

Drive and Media for PC/AT

Drive Speed (RPM)	Capacity (Kbyte)	Data Rate (Kbps)	Sector	Cyl.
300	360	250	9	40
360*	360	300	9	40
360	1.2Mbyte	500	15	80

*When a 360Kbyte diskette is in the 1.2 Mbyte drive.

IDE Interface

The 82C711/712 integrates the complete IDE interface into a single chip. The 82C711/712 IDE signals connect directly to the IDE connector. Two transceivers whose direction signals are controlled by $\overline{\text{IDEENLO}}$ and $\overline{\text{IDEENHI}}$ are required for the low byte and the high byte data.

PC/AT Task File Registers

I/O Address	Type Access	Description
1F0H	R/W	Data Register
1F1H	R	Error Register
	W	Write Precomp.
1F2H	R/W	Sector Count
1F3H	R/W	Sector Number
1F4H	R/W	Cylinder Low
1F5H	R/W	Cylinder High
1F6H	R/W	Drive/Head
1F7H	R	Status Register
	W	Command Reg.

PC/AT Alternate Registers

I/O Address	Type Access	Description
3F6H	W	Fixed Disk
3F7H	R	Digital Input

The description of these registers can be found in the IDE interface section.

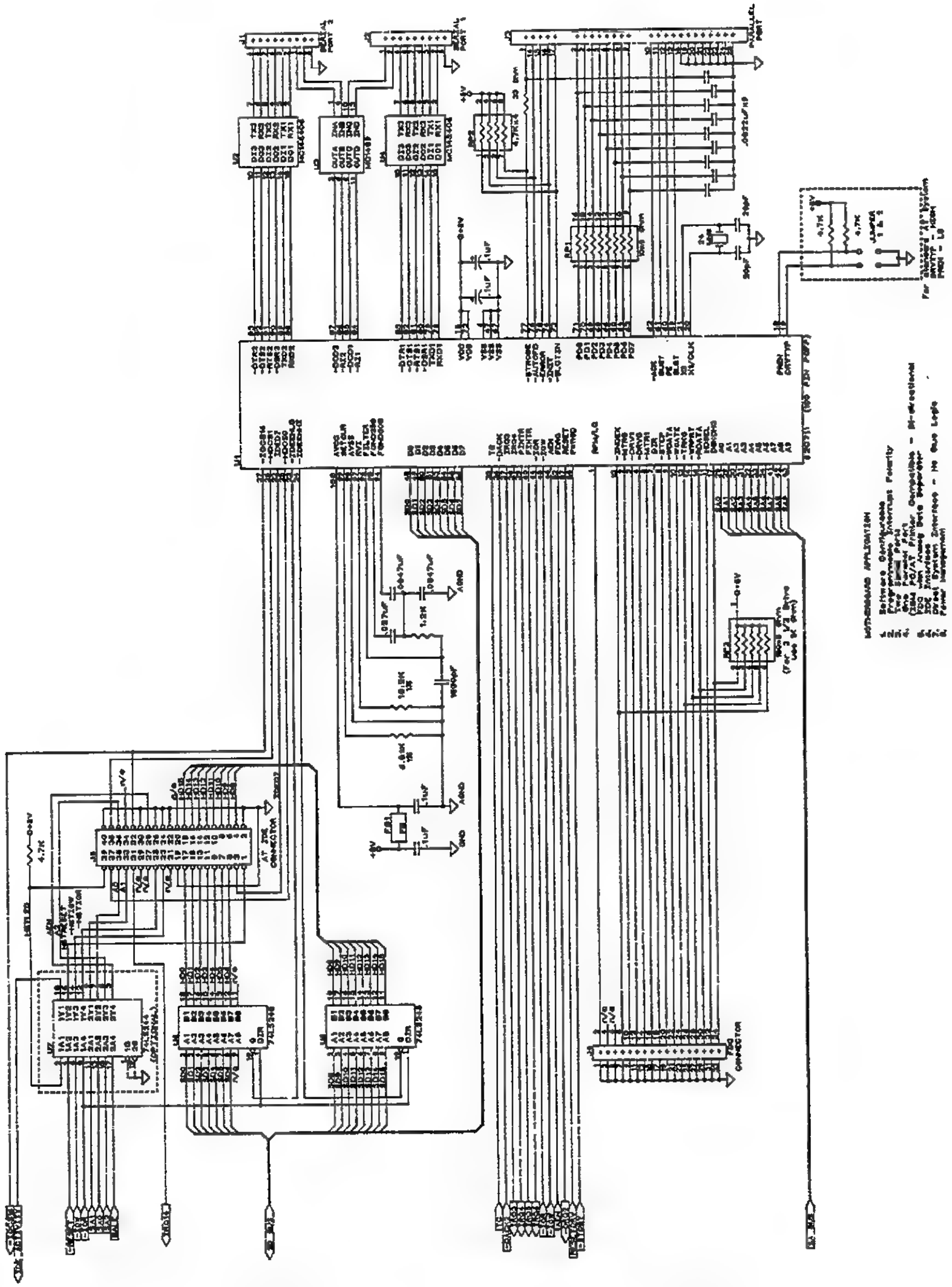


Figure 8.1 82C711 Motherboard Application

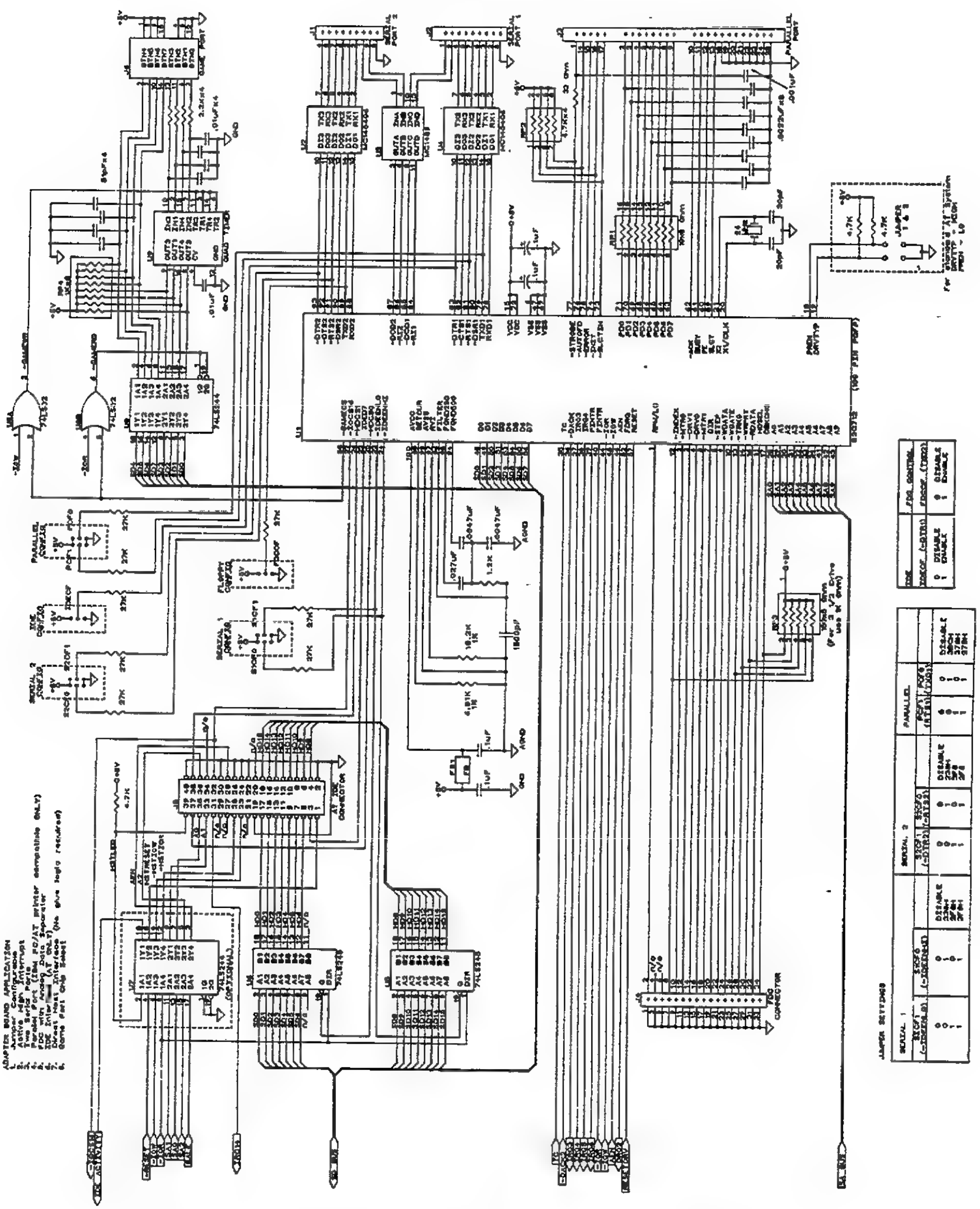


Figure 8.2 82C712 Motherboard Application

Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
Vcc	Supply Voltage	3.0		7.0	Volts
VI	Input Voltage	–0.5		5.5	Volts
TA	Operating Temperature	0		70	°C
Tstg	Storage Temperature	–40		125	°C

DC Characteristics Vcc = 5.0 ± 0.5V, Temp = 0°C to 70°C (Operating)

Type	Symbol	Min	Typ	Max	Units	Test Condition
	V_{CC}	4.5	5.0	5.5	V	
O	I_{OL}			4.0	mA	$V_{OL\ MAX} = 0.4V$
	I_{OH}			–1.0	mA	$V_{OH\ MAX} = 2.4V$
OH	I_{OL}			24	mA	$V_{OL\ MAX} = 0.5V$
	I_{OH}			–12	mA	$V_{OH\ MAX} = 2.4V$
OC	I_{OL}			24	mA	$V_{OL\ MAX} = 0.5V$
	I_{OH}			–150	µA	$V_{OH\ MAX} = 2.4V$
OD	I_{OL}			48	mA	$V_{OL\ MAX} = 0.5V$
	I_{OH}			–10	µA	$V_{OH\ MAX} = 2.4V$
OL	I_{OL}			8	mA	$V_{OL\ MAX} = 0.5V$
	I_{OH}			–10	µA	$V_{OH\ MAX} = 2.4V$
I	I_{IL}			–0.2	mA	$V_{CC\ MAX}$, $V_{IL} = 0.4V$
	I_{IH}			20	µA	$V_{CC\ MAX}$, $V_{IH} = 2.7V$
	V_{IL}			0.8	V	
	V_{IH}	2.0			V	
ICLK	I_{IL}			–0.2	mA	$V_{CC\ MAX}$, $V_{IL} = 0.4V$
	I_{IH}			20	µA	$V_{CC\ MAX}$, $V_{IH} = 2.7V$
	V_{IL}			0.4	V	
	V_{IH}	3.0			V	
IS	I_{IL}			–0.2	mA	$V_{CC\ MAX}$, $V_{IL} = 0.4V$
	I_{IH}			20	µA	$V_{CC\ MAX}$, $V_{IH} = 2.7V$
	V_{IL}			0.8	V	
	V_{IH}	2.2			V	
	hys		250		mV	
I_{STBY}				250	µA	
T	I_{OL}			24	mA	$V_{OL\ MAX} = 0.4V$
	I_{OH}			–12	mA	$V_{OL\ MIN} = 2.4V$
I_{CC}			10	40	mA	

AC ELECTRICAL CHARACTERISTICS

Symbol	Description	Min	Max	Units
Host Interface Timing				
t1	RESET width	500		ns
t2	$\overline{IOR}$, $\overline{IOW}$ width	150		ns
t3	AEN,$\overline{IOCS16}$ setup time to $\overline{IOR}$,$\overline{IOW}$	40		ns
t4	AEN,$\overline{IOCS16}$ hold time from $\overline{IOR}$,$\overline{IOW}$	10		ns
t5	Address bus setup time to $\overline{IOR}$,$\overline{IOW}$	40		ns
t26	Address bus hold time from $\overline{IOR}$,$\overline{IOW}$	10		ns
t27	Data setup time to $\overline{IOW}$	40		ns
t6	Data hold time from $\overline{IOW}$	10		ns
t7	Data bus delay from $\overline{IOR}$		100	ns
t8	Data bus hold time from $\overline{IOR}$	10	60	ns
Parallel Port Timing				
t12	PD0-PD7,$\overline{INT}$,$\overline{STROBE}$,$\overline{AUTOFD}$,$\overline{SLCTIN}$ delay from Data bus		100	ns
t13	INTR delay from $\overline{ACK}$		60	ns
IDE Interface Timing				
t14	$\overline{IDEENLO}$,$\overline{IDEENHI}$ delay from AEN,$\overline{IOCS16}$		40	ns
t15	$\overline{IDEENLO}$,$\overline{IDEENHI}$ delay from address bus		40	ns
t16	IDED7 to DATA bus bit 7 delay (READ cycle)		60	ns
t17	DATA bus bit 7 to IDED7 delay		50	ns
DMA Interface Timing				
t18	$\overline{DACK}$ setup time to $\overline{IOR}$,$\overline{IOW}$	40		ns
t19	$\overline{DACK}$ hold time from $\overline{IOR}$,$\overline{IOW}$	40		ns
t20	$\overline{DACK}$ to $\overline{IDEENLO}$,$\overline{IDEENHI}$ delay		40	ns
t21	AEN,$\overline{IOCS16}$ to $\overline{IDEENLO}$,$\overline{IDEENHI}$ delay		40	ns
Serial Port Timing				
t28	$\overline{IOW}$ to $\overline{RTS}$,$\overline{DTR}$,$\overline{OUT1}$ delay		200	ns
t22	$\overline{IOW}$ to SINTR tri-state delay	10	100	ns
t23	SINTR active delay from $\overline{CTS}$,$\overline{DSR}$,$\overline{DCD}$		100	ns
t24	SINTR inactive delay from $\overline{IOR}$ (leading edge)		120	ns
t25	SINTR inactive delay from $\overline{IOW}$ (trailing edge)		125	ns
Configuration Timing				
t29	Input setup time	50		ns
t30	Input hold time	50		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Description	Min	Typ	Max	Units	Test Condition
Write Clock						
t30 (1)	Floppy Clock cycle		125		ns	8 MHz
	Derived from 24 MHz source		208.3		ns	4.8 MHz
			250		ns	4 MHz
t31 (1)	Write clock active high		2		t30	
t32 (1)	Delay from rising FCLK to rising WCLK	0		40	ns	
t33 (1)	Delay from rising FCLK to falling WCLK	0		40	ns	
Read Operation						
t34	Read data active high	40			ns	
t35 (1)	Window hold time to read data	15			ns	
t36 (1)	Window hold time from read data	15			ns	
Write Operation						
t38 (1)	Write clock cycle		16		t30	MFM=0, 5 1/4"
			8		t30	MFM=1, 5 1/4"
			8		t30	MFM=0, 8"
			4		t30	MFM=1, 8"
			8		t30	MFM=0, 3 1/2"
			4		t30	MFM=1, 3 1/2"
t39 (1)	Write clock rise/fall time			20	ns	
t40	FCLK to $\overline{\text{WGATE}}$ delay	10		80	ns	
t41 (1)	Preshift delay from rising WCLK	10		80	ns	
t42	$\overline{\text{WDATA}}$ delay from rising FCLK	10		80	ns	
t43	$\overline{\text{WDATA}}$ width	t30-50			ns	
Seek Operation						
t44 (1)	$\overline{\text{DRV0}}$, 1 hold time to RW/seek	12			µs	8 MHz CLK (2)
t45 (1)	RW/Seek hold time to DIR	7			µs	8 MHz CLK (2)
t47 (1)	$\overline{\text{SEEK}}$ hold time to DIR	30			µs	8 MHz CLK (2)
t48	$\overline{\text{STEP}}$ active time	6	7	8	µs	8 MHz CLK (2)
t50	DIR hold time after $\overline{\text{STEP}}$	24			µs	8 MHz CLK (2)
t51	DIR hold time to $\overline{\text{STEP}}$	10			µs	8 MHz CLK (2)
t52	$\overline{\text{STEP}}$ cycle time	33			µs	8 MHz CLK (2)

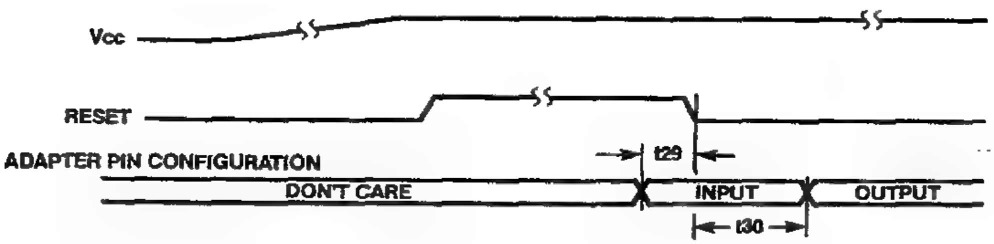
NOTE:
1. These are internal signals.
2. Double these values for a 4 MHz clock period.

AC ELECTRICAL CHARACTERISTICS (Continued)

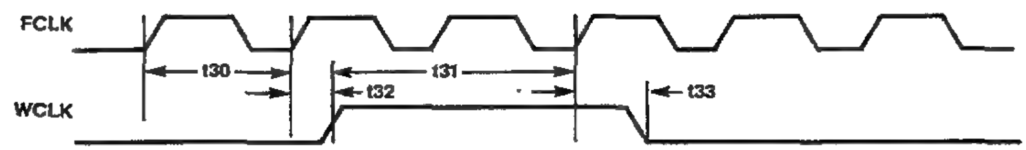
Symbol	Description	Min	Max	Units
Clock Timing				
tH	Clock high	17		ns
tL	Clock low	17		ns
tR	Clock rise time		5	ns
tF	Clock fall time		5	ns

CLOCK TIMING

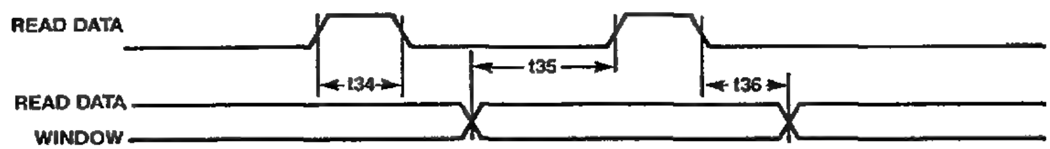
CONFIGURATION TIMING



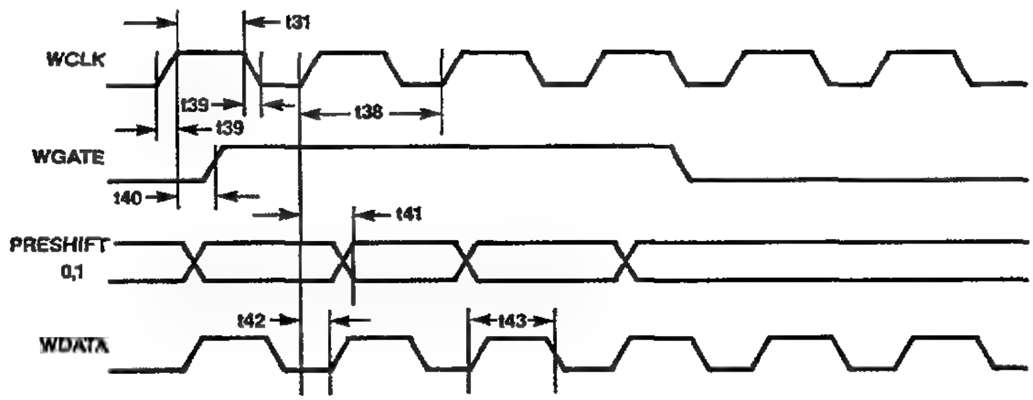
WRITE CLOCK



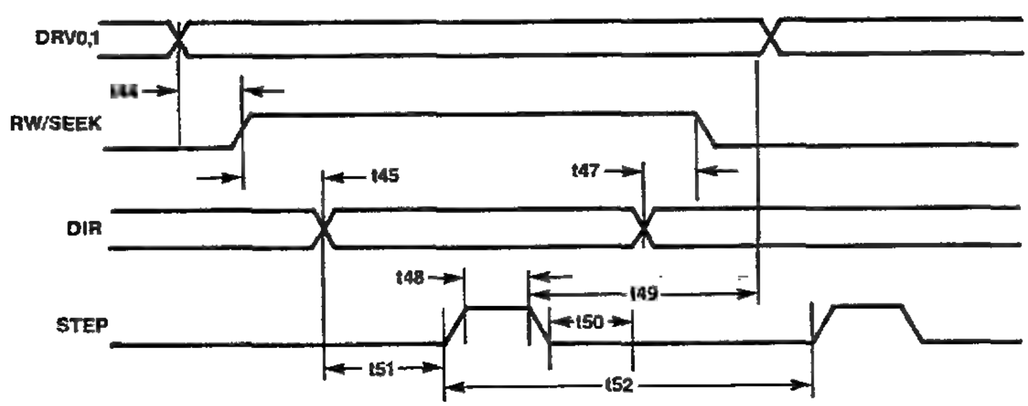
FDD READ OPERATION



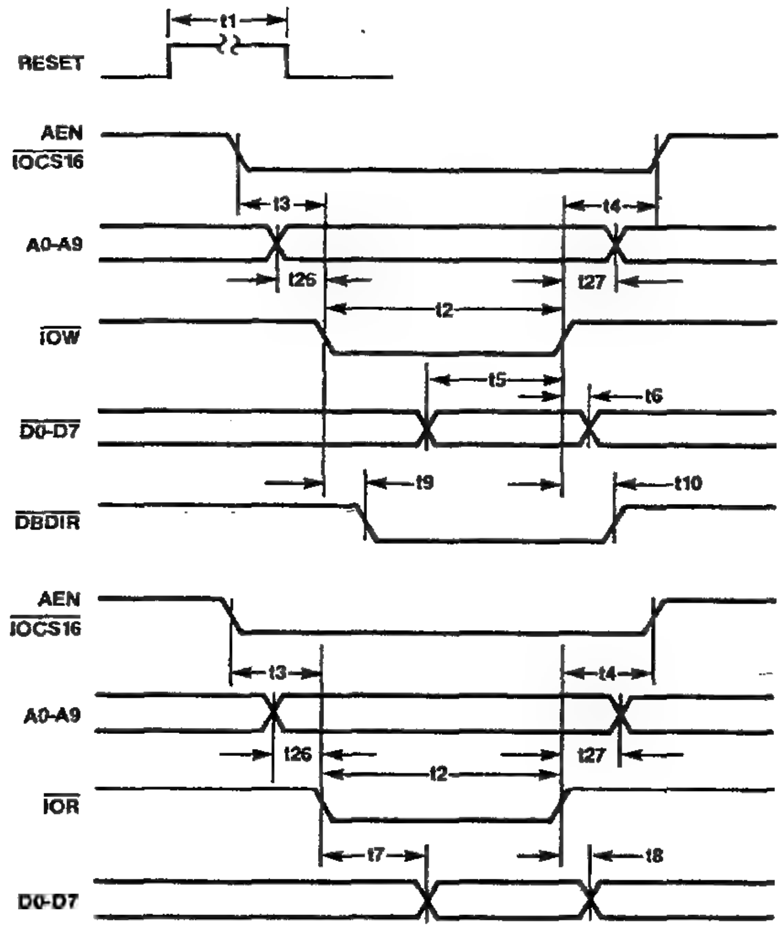
FDD WRITE OPERATION



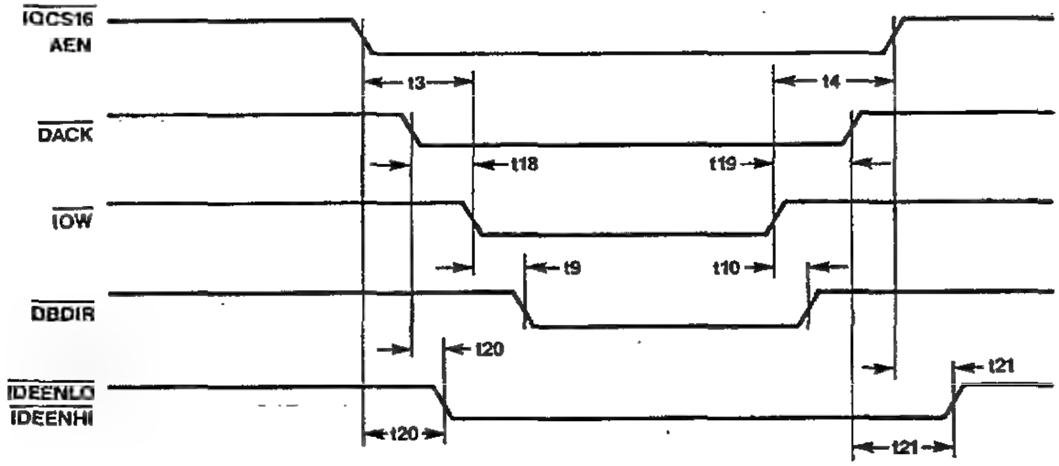
SEEK OPERATION



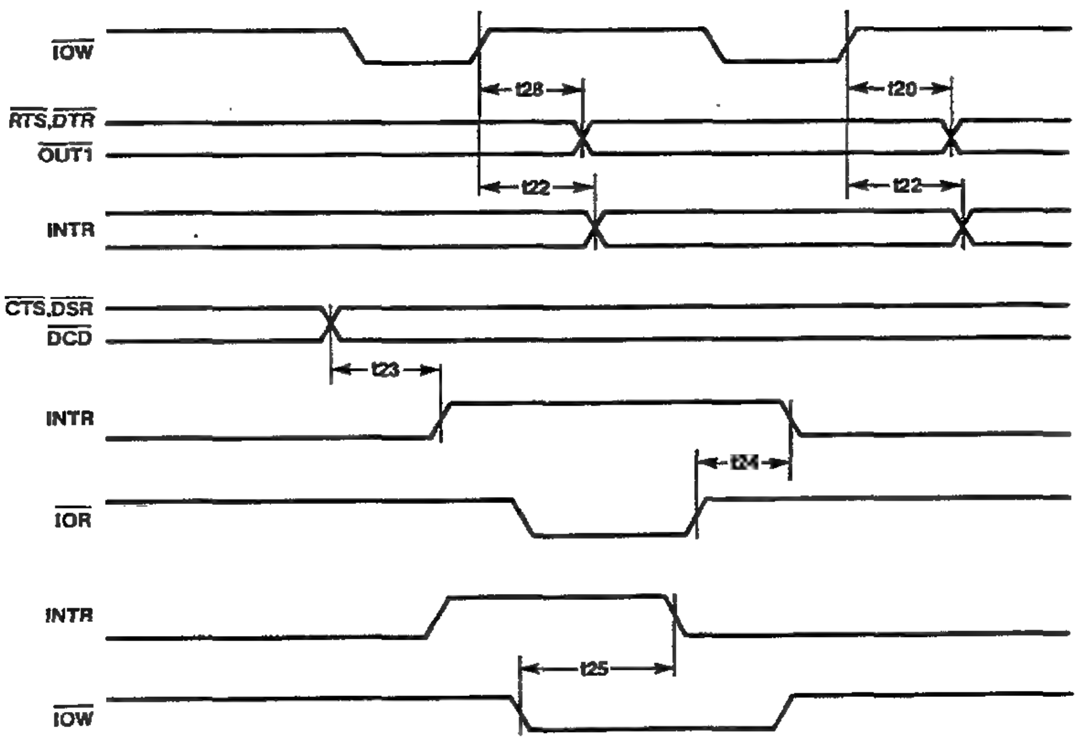
HOST INTERFACE TIMING



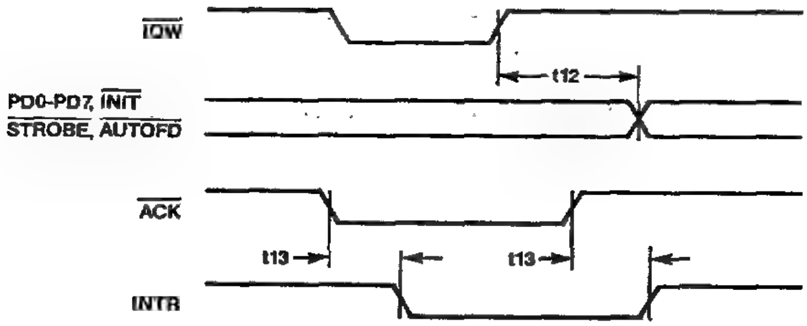
DMA TIMING



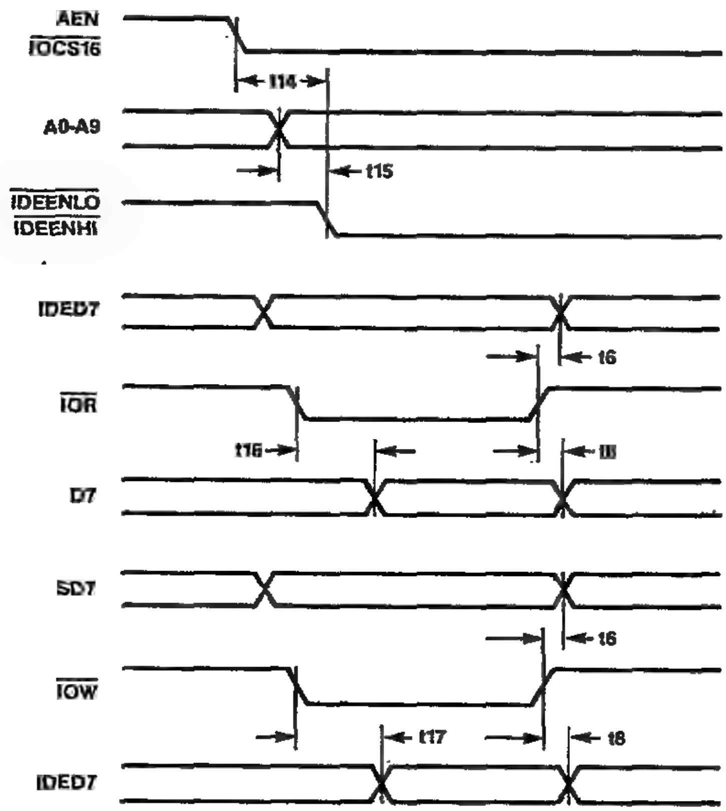
SERIAL PORT TIMING



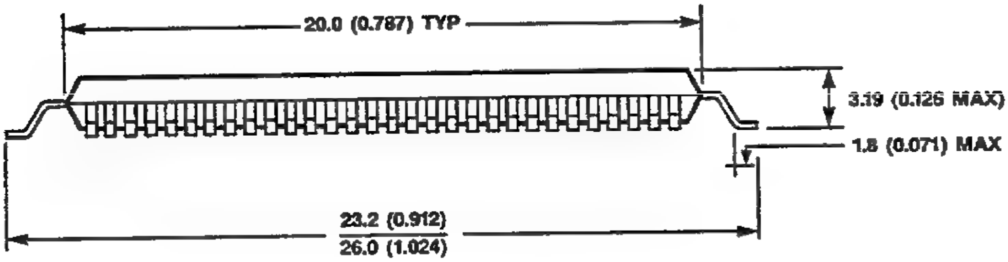
PARALLEL PORT TIMING

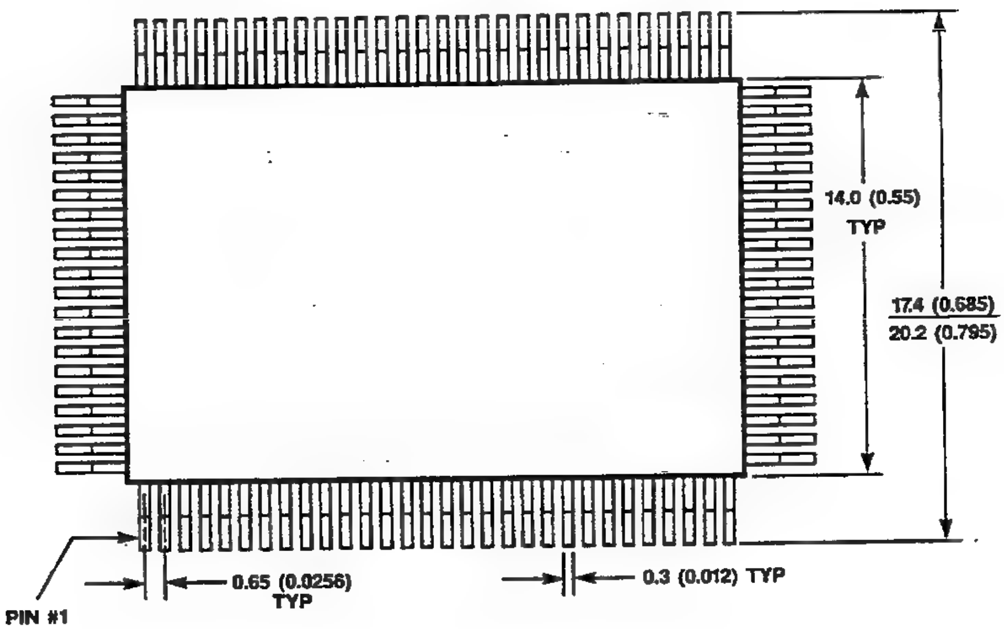


IDE INTERFACE TIMING



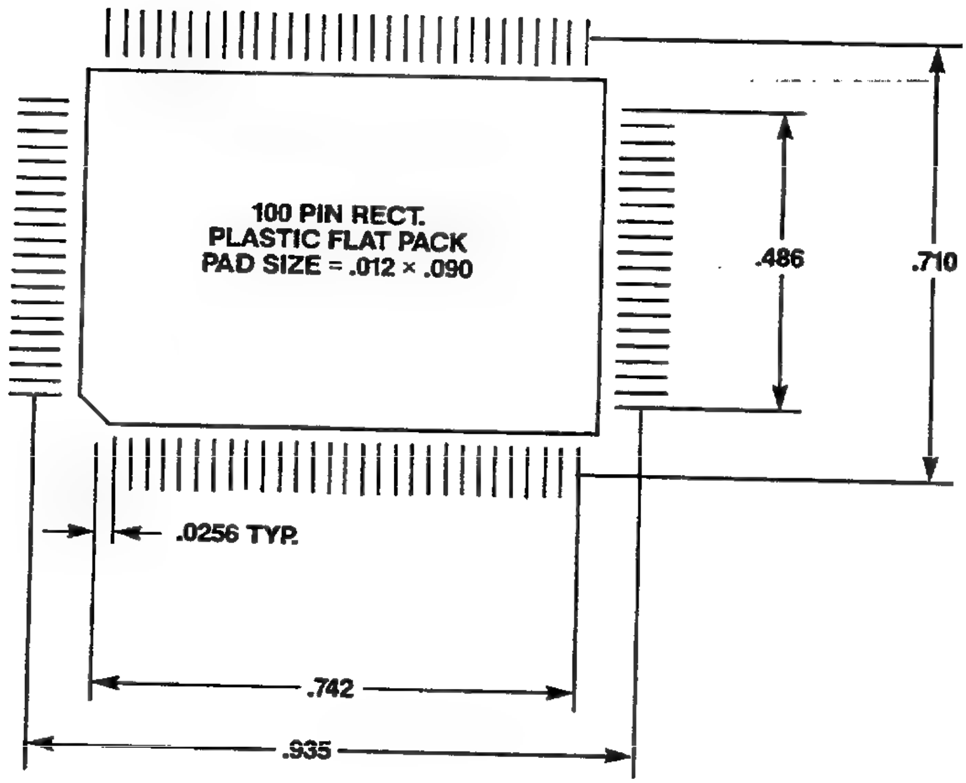
100 - PIN PLASTIC FLAT PACK (RECTANGULAR)





DIMENSIONS: mm (in)

SOLDER PAD LAYOUT DIMENSIONS



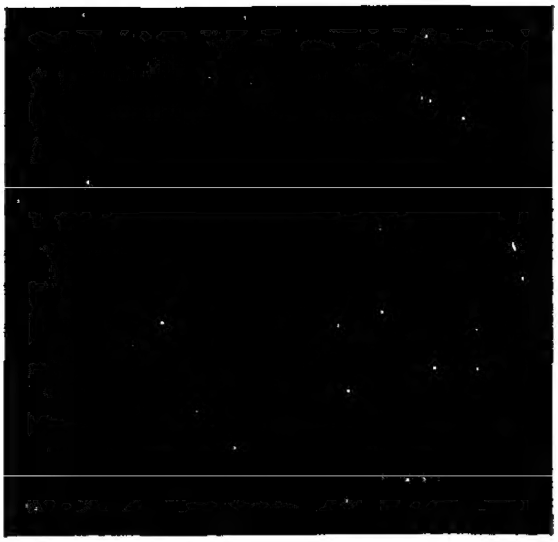
DIMENSIONS: inches

F82C711/712 (PQFP) PINOUT—100 PINS

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	RPM/LC	27	HDACK	52	FDRQ	79	PCF0
2	MTR0	27	IOCS16	53	D4	79	TXD1
3	DRV1	28	A0	54	D5	80	DSR1
4	DRV0	29	A1	55	D6	81	PCF1
5	MTR1	30	A2	56	D7	81	RTS1
6	Vss	31	A3	57	RESET	82	CTS1
7	DIR	32	A4	58	GAMECS (712)	83	DTR1
8	STEP	33	A5	58	PWRGD (711)	83	IDECF
9	WDATA	34	A6	59	SLCT	84	RI1
10	WGATE	35	TC	60	PE	85	DCD1
11	HDSEL	36	DACK	61	BUSY	86	RI2
12	INDEX	37	IRQ3	62	ACK	87	DCD2
13	TRK0	37	SSPIRQ	63	PD7	88	RXD2
14	WRPRT	38	IRQ4	64	PD6	89	TXD2
15	Vcc	38	PSPIRQ	65	PD5	89	FDCCF
16	RDATA	39	PINTR	66	PD4	90	DSR2
17	DSKCHG	40	FINTR	67	Vss	91	RTS2
18	PREN	41	A7	68	PD3	91	S2CF0
19	DRVTYP	42	A8	69	PD2	92	CTS2
20	X1/CLK	43	A9	70	PD1	93	DTR2
21	X2	44	IOR	71	PD0	93	S2CF1
22	IDED7	45	IOW	72	Vcc	94	FGND500
23	IDEENLO	46	AEN	73	SLCTIN	95	FGND250
23	S1CF1	47	Vss	74	INIT	96	FILTER
24	IDEENHI	48	D0	75	ERROR	97	RVI
24	S1CF0	49	D1	76	AUTOFD	98	AVss
25	HDCS0	50	D2	77	STROBE	99	SETCUR
26	HDCS1	51	D3	78	RXD1	100	AVcc

F82C711/712 (PQFP) PINOUT—100 PINS

NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN
A0	28	DCD2	87	IOCS16	27	RTS2	91
A1	29	DIR	7	IOR	44	RVI	97
A2	30	DRV0	4	IOW	45	RXD1	78
A3	31	DRV1	3	IRQ3	37	RXD2	88
A4	32	DRVTYP	19	IRQ4	38	S1CF0	24
A5	33	DSKCHG	17	MTR0	2	S1CF1	23
A6	34	DSR1	80	MTR1	5	S2CF0	91
A7	41	DSR2	90	PCF0	79	S2CF1	93
A8	42	DTR1	83	PCF1	81	SETCUR	99
A9	43	DTR2	93	PD0	71	SLCT	59
ACK	62	ERROR	75	PD1	70	SLCTIN	73
AEN	46	FDCCF	89	PD2	69	SSPIRQ	37
AUTOFD	76	FDRQ	52	PD3	68	STEP	8
AVcc	100	FGND250	95	PD4	66	STROBE	77
AVss	98	FGND500	94	PD5	65	TC	35
BUSY	61	FILTER	96	PD6	64	TRK0	13
CTS1	82	FINTR	40	PD7	63	TXD1	79
CTS2	92	GAMECS (712)	58	PE	60	TXD2	89
D0	48	HDACK	27	PINTR	39	Vcc	15
D1	49	HDCS0	25	PREN	18	Vcc	72
D2	50	HDCS1	26	PSPIRQ	38	Vss	6
D3	51	HDSEL	11	PWRGD (711)	58	Vss	47
D4	53	IDECF	83	RDATA	16	Vss	67
D5	54	IDED7	22	RESET	57	WDATA	9
D6	55	IDEENHI	24	RI1	84	WGATE	10
D7	56	IDEENLO	23	RI2	86	WRPRT	14
DACK	36	INDEX	12	RPM/LC	1	X1/CLK	20
DCD1	85	INIT	74	RTS1	81	X2	21



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